



**...CALL FOR PAPERS and
Session Chairs...
2nd Annual iMAPS
Advanced Technology Workshop**

**FUTURE DIGITAL INTERCONNECTS
OVER 1,000 MHz**

January 17-18, 2000

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MESSAGE FROM THE CHAIRS

High Speed Digital Interconnects are becoming an increasingly important part of new product development. What are the implications for all levels of packaging?

IMAPS' 2nd Annual Advanced Technical Workshop (ATW) on this topic wishes to outline the problem for future developments.

Future microprocessors will have on-chip clock speeds of > 1,000 MHz, off chip clock speeds of 100's of MHz, with 1,000's of I/O's dissipating 100's of watts.

This new reality challenges the design, materials, packaging, manufacturing, assembly and test community to manage high speed digital signal integrity like never before.

The tradeoffs for clear signal integrity of decoupling capacitance, attenuation, density, thermal management, cost, time to market are all daunting.

This IMAPS (ATW) will bring together a diverse group of professionals from all disciplines to define the state of the art and identify gaps which need filling.

PROPOSED SESSION TOPICS

- SYSTEM ISSUES – Define the Problem
- MODELING
- DESIGN TOOLS
- MATERIALS ISSUES
- PACKAGING -- FROM DRIVER TO RECEIVER (1st, 2nd and 3rd level)
- CONNECTORS
- EMI/SHIELDING ISSUES
- INTEGRATED PASSIVES
- CASE STUDIES
- NOVEL DESIGN CONCEPTS

DEADLINES

Short abstracts	October 15, 1998
Final program	Nov 1, 1998
Extended abstracts	December 15, 1998