

# MB87001A

## CMOS PLL FREQUENCY SYNTHESIZER

### CMOS SERIAL INPUT PHASE-LOCKED-LOOP (PLL) FREQUENCY SYNTHESIZER

The Fujitsu MB87001A, fabricated in CMOS technology, is a serial input PLL frequency synthesizer.

The MB87001A contains an inverter for connection to an external oscillator, a programmable reference divider, a divide factor of programmable reference divider control circuit, a phase detector, a charge pump, a 17-bit shift register, a 17-bit latch, a programmable divider (a binary 7-bit swallow counter, a binary 10-bit programmable counter), and a control generator for an external dual modulus prescaler.

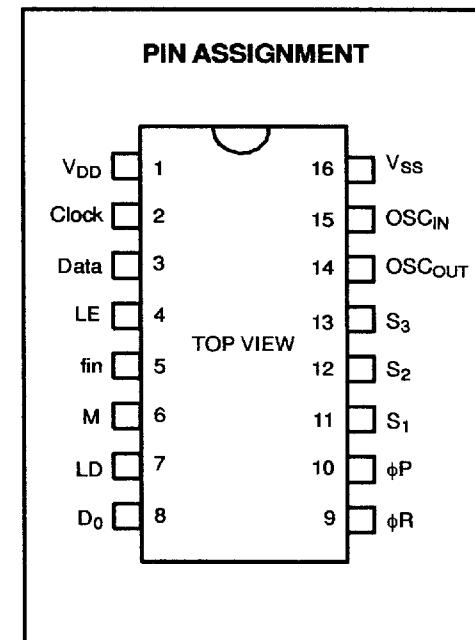
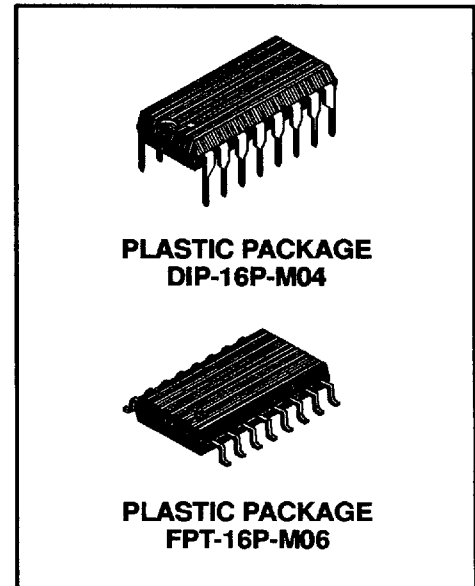
When supplemented with a loop filter and VCO, the MB87001A contains the necessary circuitry to make up a Phase Locked Loop (PLL). Typically, a dual modulus prescaler such as the MB501L can be added, allowing input frequency operation up to 1.1 GHz.

- Single power supply voltage:  
 $V_{DD} = 2.7V$  to  $5.5V$
- Wide temperature range:  
 $T_A = -40$  to  $85^\circ C$
- 13MHz typical input capability  
@5V (fin input)
- On-chip inverter for oscillator
- 8 divide factors for programmable reference divider is selected by  $S_1$ ,
- $S_2$  and  $S_3$  input (1/8, 1/16, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048)
- Programmable 17-bit divider with input amplifier consisting of:  
Binary 7-bit swallow counter  
Binary 10-bit programmable counter
- 2 type of phase detector output  
On-chip charge pump output  
Output for external charge pump
- Easy interface to Fujitsu dual modulus prescaler

### ABSOLUTE MAXIMUM RATINGS (see NOTE) ( $V_{SS} = 0V$ )

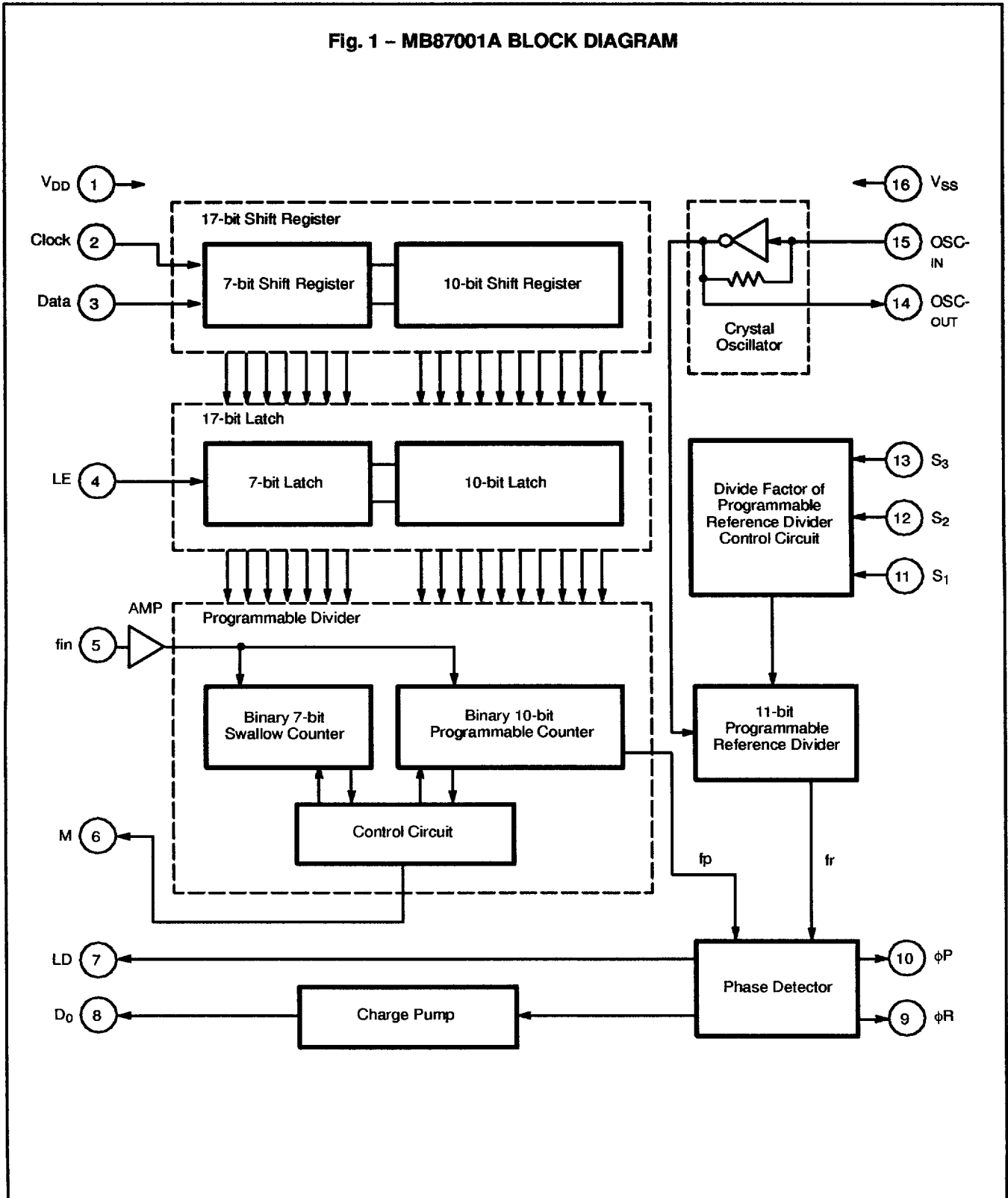
Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{DD}$	$V_{SS} - 0.5$ to $V_{SS} + 7.0$	V
Input Voltage	$V_{IN}$	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
Output Voltage	$V_{OUT}$	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
Output Current	$I_{OUT}$	$\pm 10$	mA
Open-drain Output	$V_{OOP}$	$V_{SS} - 0.5$ to $V_{DD} + 3.0$	V
Operating Temperature	$T_A$	$-40$ to $+85$	$^\circ C$
Storage Temperature	$T_{STG}$	$-65$ to $+150$	$^\circ C$
Power Dissipation	$P_D$	300	mW

**NOTE:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 - MB87001A BLOCK DIAGRAM



## PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	V <sub>DD</sub>	-	Power supply voltage input.
2	Clock	I	Clock signal input for 17-bit shift register. Each rising edge of the clock shifts one bit of the data into the shifter register.
3	Data	I	Serial data input for 17-bit shift register. The data is used for setting the divide factor of programmable divider.
4	LE	I	Load enable input. When this pin is high level (high active), the data stored in the 17-bit shift register is transferred to 17-bit latch.
5	fin	I	Input for programmable divider from VCO or prescaler output. This input involves bias circuit and amplifier. The connection with external dual modulus prescaler should be an AC connection.
6	M	O	Control output for external dual modulus prescaler. The connection to the prescaler should be DC connection. This output level is synchronized with falling edge of fin input signal (pin #5). Pulse Swallow Function: MB501L      M = High: Preset modulus factor 64 or 128 M = Low: Preset modulus factor 65 or 129
7	LD	O	Output of phase detector. It is high level when fr and fp are equal, and then the loop is locked. Otherwise it outputs negative pulse signal.
8	D <sub>O</sub>	O	Three-state charge pump output of the phase detector. The mode of D <sub>O</sub> is changed by the combination of programmable reference divider output frequency fr and programmable divider output frequency fp as listed below: fr > fp:      Drive mode (D <sub>O</sub> = High level) fr = fp:      High-impedance mode fr < fp:      Sink mode (D <sub>O</sub> = Low level)
9 10	φR φP	O O	Phase detector outputs for an external charge pump. The mode of φR and φP are changed by the combination of programmable reference divider output frequency fr and programmable divider output frequency fp as listed below: φR                      φP fr > fp:      Low                      Low fr = fp:      Low                      High-Impedance fr < fp:      High                      High-Impedance * φP is a N-channel open drain output.

## PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Description																																				
11 12 13	S <sub>1</sub> S <sub>2</sub> S <sub>3</sub>	I I I	<p>Control input for programmable reference divider. The combination of these inputs provides 8 kinds of divide factor for the programmable reference divider.</p> <table border="1"> <thead> <tr> <th>Divide Factor S<sub>n</sub></th> <th><math>\frac{1}{8}</math></th> <th><math>\frac{1}{16}</math></th> <th><math>\frac{1}{64}</math></th> <th><math>\frac{1}{128}</math></th> <th><math>\frac{1}{256}</math></th> <th><math>\frac{1}{512}</math></th> <th><math>\frac{1}{1024}</math></th> <th><math>\frac{1}{2048}</math></th> </tr> </thead> <tbody> <tr> <td>S<sub>1</sub></td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>S<sub>2</sub></td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>S<sub>3</sub></td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	Divide Factor S <sub>n</sub>	$\frac{1}{8}$	$\frac{1}{16}$	$\frac{1}{64}$	$\frac{1}{128}$	$\frac{1}{256}$	$\frac{1}{512}$	$\frac{1}{1024}$	$\frac{1}{2048}$	S <sub>1</sub>	0	1	0	1	0	1	0	1	S <sub>2</sub>	0	0	1	1	0	0	1	1	S <sub>3</sub>	0	0	0	0	1	1	1	1
Divide Factor S <sub>n</sub>	$\frac{1}{8}$	$\frac{1}{16}$	$\frac{1}{64}$	$\frac{1}{128}$	$\frac{1}{256}$	$\frac{1}{512}$	$\frac{1}{1024}$	$\frac{1}{2048}$																															
S <sub>1</sub>	0	1	0	1	0	1	0	1																															
S <sub>2</sub>	0	0	1	1	0	0	1	1																															
S <sub>3</sub>	0	0	0	0	1	1	1	1																															
14	OSC <sub>OUT</sub>	O	<p>Output pin for crystal oscillator. Output of the inverting amplifier. This pin should be open when an external oscillator is used.</p>																																				
15	OSC <sub>IN</sub>	I	<p>Input pin for crystal oscillator. Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupled when an external oscillator is used. For large amplitude signals (standard CMOS levels) DC coupling may also be used.</p>																																				
16	V <sub>SS</sub>	-	Ground																																				

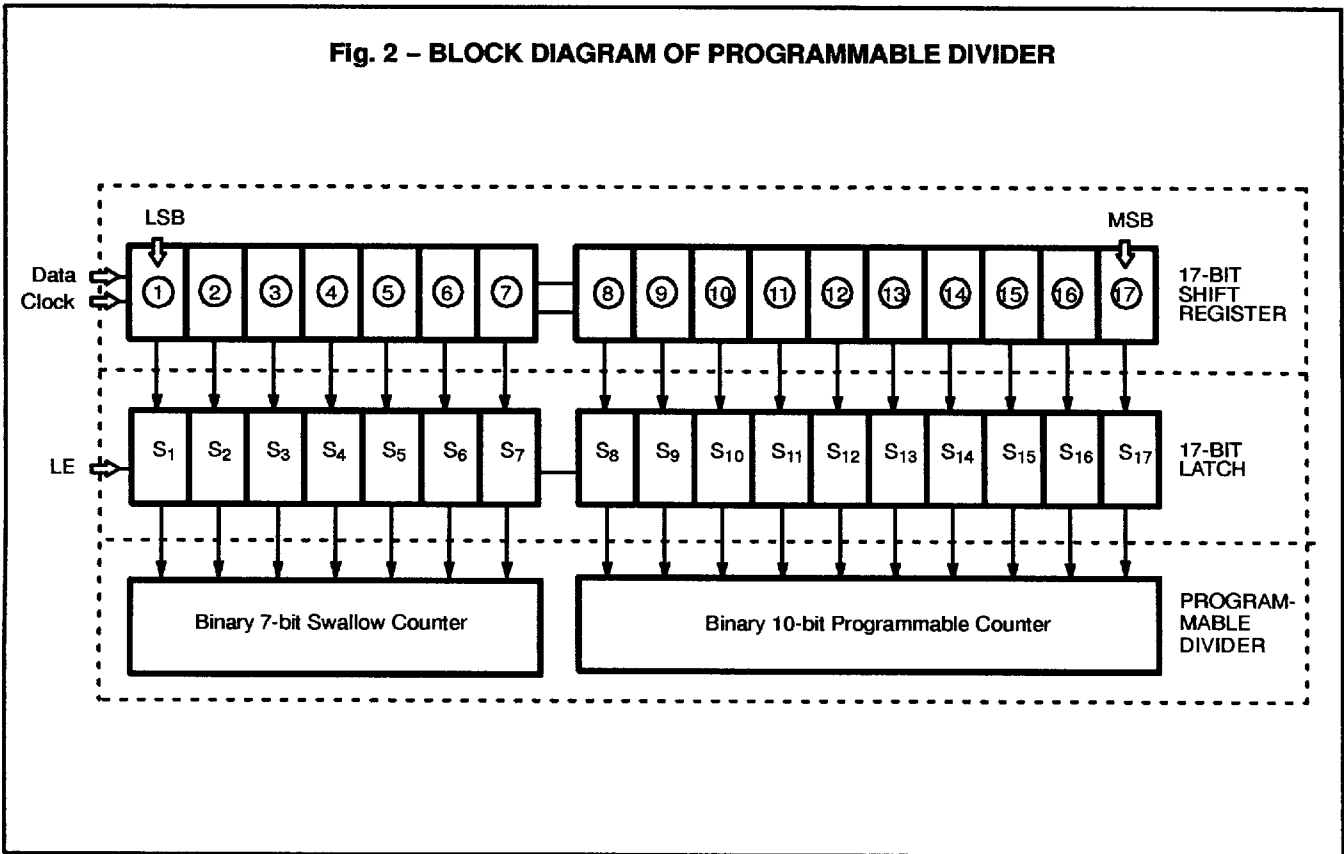
# FUNCTIONAL DESCRIPTION

## DIVIDE FACTOR OF PROGRAMMABLE DIVIDER

Serial data of binary code is input to Data pin. These data are loaded into the 17-bit shift register from MSB. When load enable signal LE is high, the data stored in the 17-bit shift register is transferred to the 17-bit latch.

The data ① to ⑦ set a divide factor of the binary 7-bit swallow counter and data ⑧ to ⑰ set a divide factor of binary 10-bit programmable counter. In other words, serial data is equivalent to the divide factor of programmable divider.

Fig. 2 - BLOCK DIAGRAM OF PROGRAMMABLE DIVIDER



**Binary 7-bit Swallow Counter Data Input**

⑦	⑥	⑤	④	③	②	①	Divide Factor A
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
·	·	·	·	·	·	·	·
1	1	1	1	1	1	1	127

**Note:** Divide factor A: 0 to 127  
 Depending upon the divide factor set input (SW) of external prescaler, the input data should be as follows.  
 Example MB501L  
 SW = H (64/65): Bit 7 of shift register (7) should be zero.

**Binary 10-bit Programmable Counter Data Input**

⑰	⑱	⑮	⑭	⑬	⑫	⑪	⑩	⑨	⑧	Divide Factor N
0	0	0	0	0	0	0	1	0	1	5
0	0	0	0	0	0	0	1	1	0	6
0	0	0	0	0	0	0	1	1	1	7
·	·	·	·	·	·	·	·	·	·	·
1	1	1	1	1	1	1	1	1	1	1023

**Note:** Divide factor less than 5 is prohibited.  
 Divide factor N: 5 to 1023

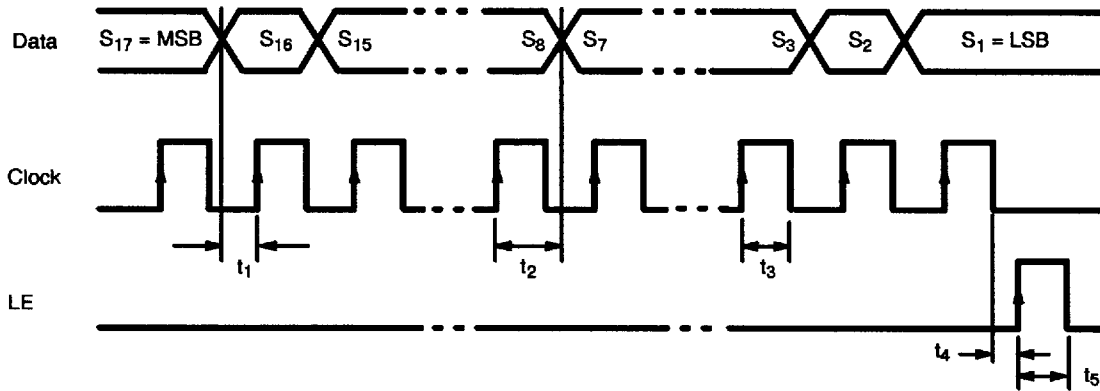
**PULSE SWALLOW FUNCTION**

$$f_{VCO} = [(N \times M) + A] \times f_r$$

- $f_{VCO}$  : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide factor of binary 10-bit programmable counter (5 to 1023)
- M : Preset modulus factor of external dual modulus prescaler (e.g. 64 in 64/65 mode, 128 in 128/129 mode of an MB501L prescaler)
- A : Preset divide factor of binary 7-bit swallow counter (0 to 127)
- $f_r$  : Output frequency of the programmable reference divider

**TIMING CHART**

•  $t_1 \sim t_5 \geq 1\mu s$ ,



**Clock** : Clock signal input for the 17-bit shift register.

Each rising edge of the clock shifts one bit of data into the shift register.

**Data** : Serial data input for the 17-bit shift register.

**LE** : Load enable input.

When LE is high (high active), the data stored in the 17-bit shift register is transferred to the 17-bit latch.

The 17-bit data is used for setting a divide factor of the programmable divider.

**RECOMMENDED OPERATING CONDITIONS**

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V <sub>DD</sub>	2.7		5.5	V
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub>		V <sub>DD</sub>	V
Operating Temperature	T <sub>A</sub>	-40		+85	°C

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## ELECTRICAL CHARACTERISTICS

 $(V_{DD} = 3.0V, V_{SS} = 0V, T_A = -40 \text{ to } 85^\circ\text{C})$ 

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
High-level Input Voltage	Except $\phi_{IN}$ and $OSC_{IN}$	$V_{IH}$	2.1			V
Low-level Input Voltage		$V_{IL}$			0.9	
Input Sensitivity	$\phi_{IN}$	$V_{\phi_{IN}}$	Amplitude in AC coupling, sine wave	0.8		$V_{P-P}$
	$OSC_{IN}$	$V_{OSC}$		1.0		
High-level Input Current	Except $\phi_{IN}$ and $OSC_{IN}$	$I_{IH}$	$V_{IN} = V_{DD}$	1.0		$\mu A$
Low-level Input Current		$I_{IL}$	$V_{IN} = V_{SS}$		-1.0	
Input Current	$\phi_{IN}$	$I_{\phi_{IN}}$	$V_{IN} = V_{SS} \text{ to } V_{DD}$		$\pm 30$	$\mu A$
	$OSC_{IN}$	$I_{OSC}$	$V_{IN} = V_{SS} \text{ to } V_{DD}$		$\pm 30$	
High-level Output Voltage	Except $\phi_P$ and $OSC_{OUT}$	$V_{OH}$	$I_{OH} = 0\mu A$	2.95		V
Low-level Output Voltage		$V_{OL}$	$I_{OL} = 0\mu A$		0.05	
Low-level Output Voltage	$\phi_P$	$V_{OLP}$	$I_{OL} = 0.8mA$		0.8	V
High-level Output Voltage	$OSC_{OUT}$	$V_{OHX}$	$I_{OH} = 0\mu A$	2.50		
Low-level Output Voltage		$V_{OLX}$	$I_{OL} = 0\mu A$		0.50	
High-level Output Current	Except $\phi_P$ and $OSC_{OUT}$	$I_{OH}$	$V_{OH} = 2.0V$	-0.5		mA
Low-level Output Current		$I_{OL}$	$V_{OL} = 0.8V$	0.5		
N-channel Open Drain Cut Off Current	$\phi_P$	$I_{OFF}$	$V_O = V_{DD} + 3.0$		1.0	$\mu A$
Power Supply Current*1		$I_{DD}$			2.0	mA
Max. Operating Frequency of Programmable Reference Divider		$f_{maxd}$		13	20	MHz
Max. Operating Frequency of Programmable Divider		$f_{maxp}$		10	20	MHz

Note: \*1:  $\phi_{IN} = 5.0MHz, 12.8MHz$  Crystal is connected between  $OSC_{IN}$  and  $OSC_{OUT}$ .  
Inputs are connected to ground except for  $\phi_{IN}$  and  $OSC_{IN}$ . Outputs are open.



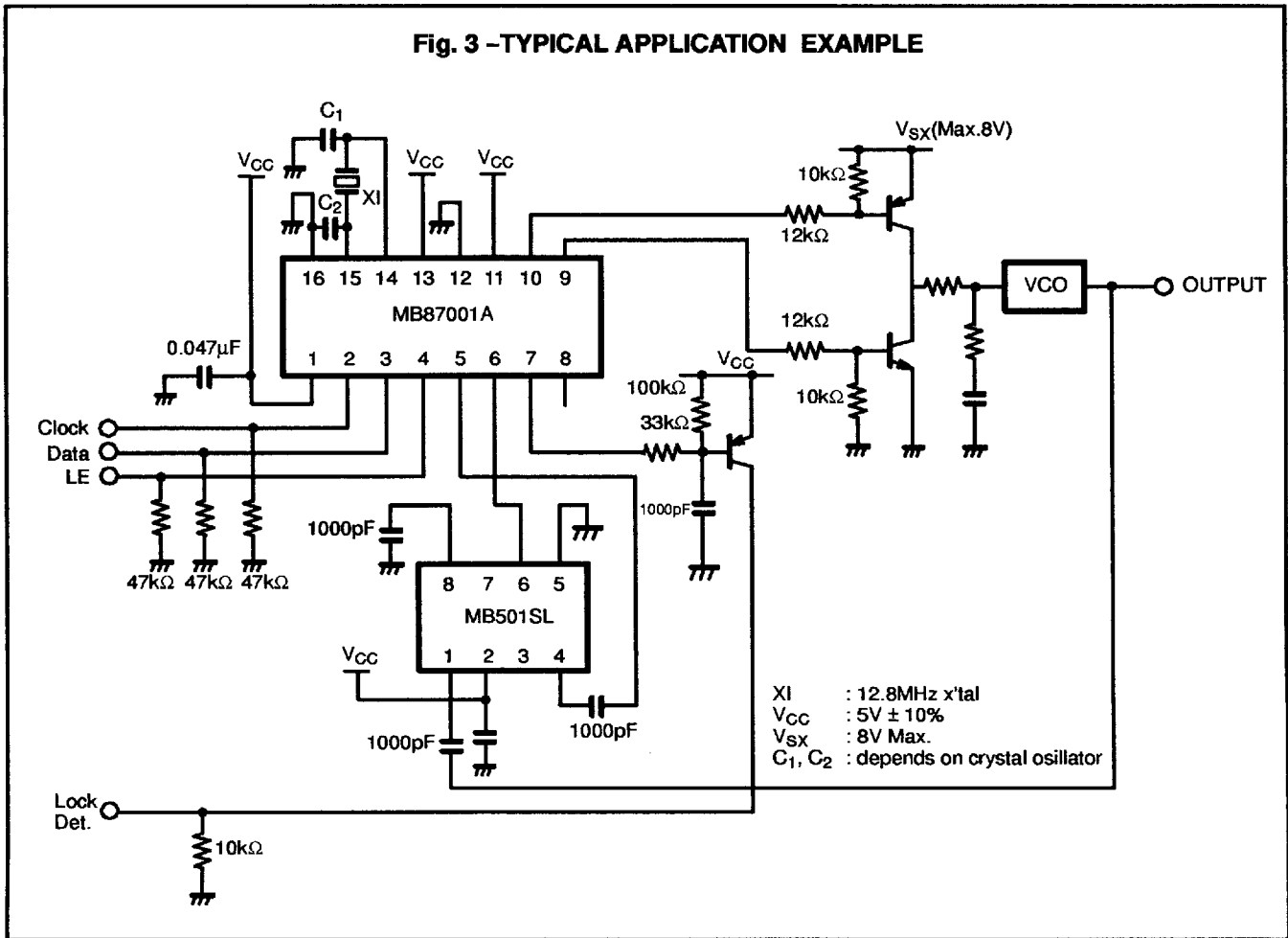
## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>DD</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -40 to 85°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
High-level Input Voltage	Except fin and OSC <sub>IN</sub>	V <sub>IH</sub>	3.5			V
Low-level Input Voltage		V <sub>IL</sub>			1.5	
Input Sensitivity	fin	V <sub>fin</sub>	Amplitude in AC coupling, sine wave	1.0		V <sub>P-P</sub>
	OSC <sub>IN</sub>	V <sub>osc</sub>		1.5		
High-level Input Current	Except fin and OSC <sub>IN</sub>	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>DD</sub>		1.0	μA
Low-level Input Current		I <sub>IL</sub>	V <sub>IN</sub> = V <sub>SS</sub>		-1.0	
Input Current	fin	I <sub>fin</sub>	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>DD</sub>		±50	μA
	OSC <sub>IN</sub>	I <sub>osc</sub>	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>DD</sub>		±50	
High-level Output Voltage	Except φP and OSC <sub>OUT</sub>	V <sub>OH</sub>	I <sub>OH</sub> = 0μA	4.95		V
Low-level Output Voltage		V <sub>OL</sub>	I <sub>OL</sub> = 0μA			
Low-level Output Voltage	φP	V <sub>OLP</sub>	I <sub>OL</sub> = 2mA			1.0
High-level Output Voltage	OSC <sub>OUT</sub>	V <sub>OHX</sub>	I <sub>OH</sub> = 0μA	4.50		V
Low-level Output Voltage		I <sub>OLX</sub>	I <sub>OL</sub> = 0μA			
High-level Output Current	Except φP and OSC <sub>OUT</sub>	I <sub>OH</sub>	V <sub>OH</sub> = 4.0V	-1.0		mA
Low-level Output Current		I <sub>OL</sub>	V <sub>OL</sub> = 0.8V	1.0		
N-channel Open Drain Cut Off Current	φP	I <sub>OFF</sub>	V <sub>O</sub> = V <sub>DD</sub> +3.0		1.0	μA
Power Supply Current*1		I <sub>DD</sub>			3.0	mA
Max. Operating Frequency of Programmable Reference Divider		f <sub>maxd</sub>		15	25	MHz
Max. Operating Frequency of Programmable Divider		f <sub>maxp</sub>		13	25	MHz

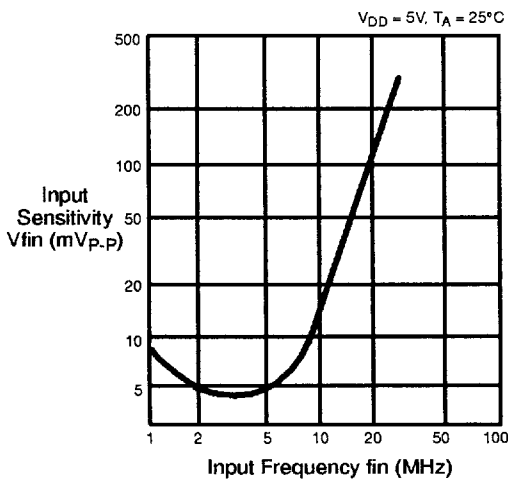
Note:\*1: fin = 5.0MHz, 12.8MHz Crystal is connected between OSC<sub>IN</sub> and OSC<sub>OUT</sub>. Inputs are connected to ground except for fin and OSC<sub>IN</sub>. Outputs are open.

Fig. 3 -TYPICAL APPLICATION EXAMPLE

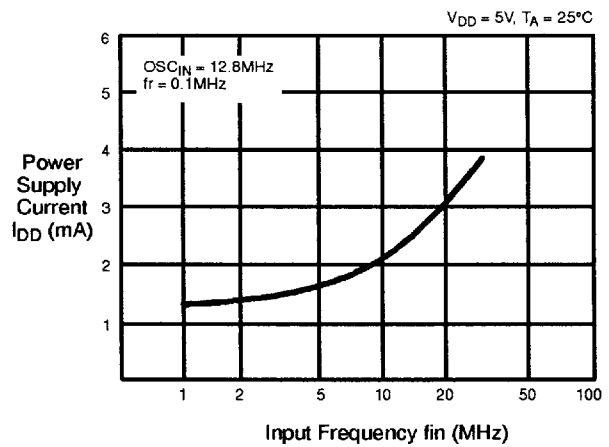


## TYPICAL CHARACTERISTICS CURVES

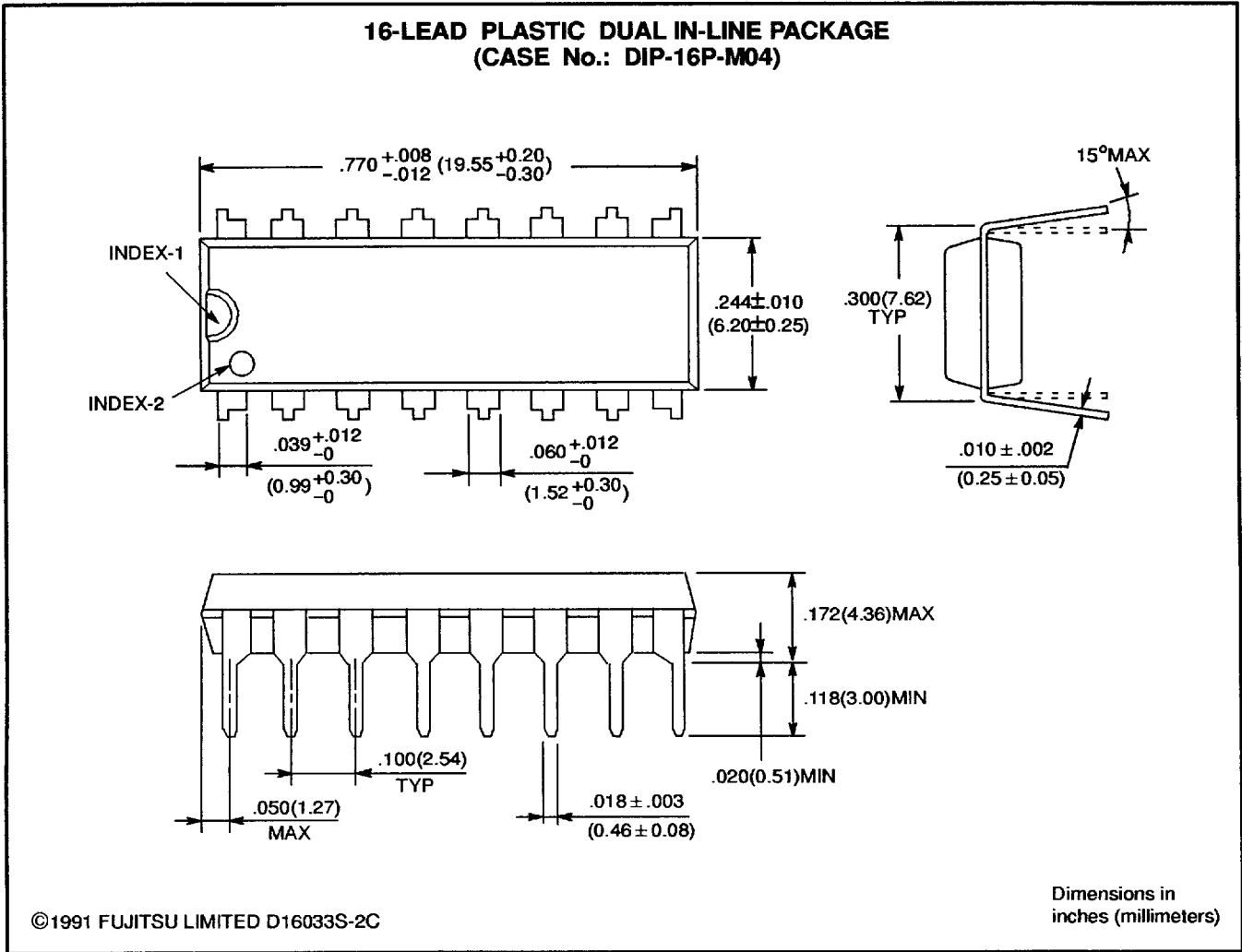
Input Sensitivity vs. Input Frequency (fin Section)



Power Supply Current vs. Input Frequency



# PACKAGE DIMENSIONS



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# PACKAGE DIMENSIONS (Continued)

