Technical Brief
AN142 Rev A3

THE POCSAG PAGING PROTOCOL

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Overview

The POCSAG name comes from the UK, and stands for: Post Office Code Standardization Advisory Group which at one time controlled all telecommunications in Britain. POCSAG is a radio data transmission protocol used to transmit one-way messages to "pagers". Pagers are radio small receivers that are activated when a properly message encoded is transmitted to them over a radio channel.

The POCSAG protocol was a major improvement over previous tone-based paging protocols, allowing for much longer pager battery life and many more subscribers per system.

There are three standard POCSAG data rates: 512, 1200, or 2400 bps. 512bps has the longest communication range, while 1200 and 2400 allow for more pages to be transmitted per second.

POCSAG pages are transmitted in a batch structure, with a long pre-amble at the beginning of the message to allow pagers to periodically asynchronously wake up, and listen for a page. Once they detect the preamble, they sync-up to the PCSAG message by detecting the embedded synch bits. Pagers analyze sequential batches of pages to see if any batch contains an address code word frame with its own cap code.

Modulation

The typical over-the-air modulation used is RF Frequency Shift Keying (FSK) with a ±4500Hz shift on the RF carrier. The high frequency represents a digital 0 and the low frequency a digital 1. Often single transmission channels contain blocks of data at more than one of the rates.

CAP Codes

"Cap Code" stands for Channel Access Protocol code, which is the unique ID code assigned to a particular pager.

When a pager detects its own cap code within a POCSAG address frame, it will alert the user with a beep, tone, or vibration. And if it has display capability, it will display a number if it is a numeric pager, or display a text message if it is an alpha-numeric pager. POCSAG cap codes are 21 bits long, allowing for up to 2097152 unique cap codes per radio channel. The cap code is comprised of 18 address bits and 3 frame location bits. The frame location

bits are the least-significant bits, and the address bits are the most-significant bits of the cap code.

The POCSAG Transmission Format

A POCSAG transmission consists of a 576 bit preamble and one or more batches of code words. Each batch contains:

- A 32-bit frame synchronization code (FSC) that marks the start of a code word batch
- Eight address frames of two 32-bit addresses or idle code words each.

The sync and code words are transmitted Most Significant Bit first, LSB last.

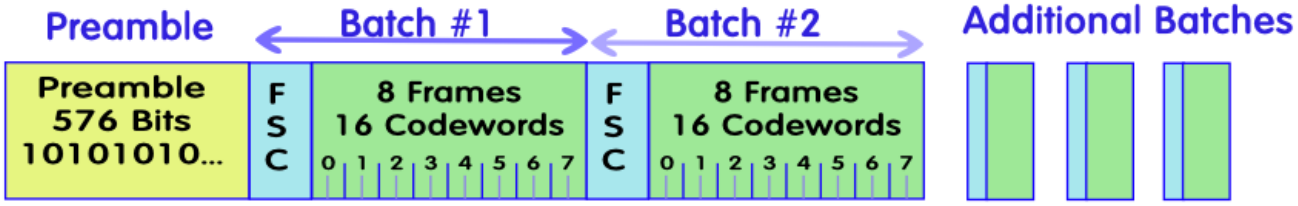
The Preamble

The preamble consists of 576 bits of alternating 1-0 bits transmitted. To save power, most paging receivers and pagers put themselves to sleep, drawing very little power, and periodically wake-up to listen on the radio channel for a POCSAG preamble.

When a receiver detects the presence of preamble, to stays awake, and synchronizes its receiver to the bit-rate of the preamble. The alternating 1-0 pattern of the preamble identifies the data-rate of the upcoming paging batches. All batches after the preamble are sent at the same data rate of either 512, 1200, or 2400 bits per second.

POCSAG Batches

A POCSAG starts with a frame synchronization code (FSC) followed by 8 frames. Each of the 8 frames has two code words in it. Up to 16 address code words may be sent per batch. For proper batch structure, each frame has two address code words, two idle code words, or two message code words.



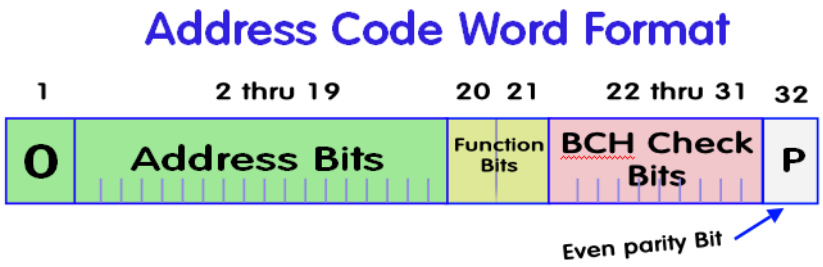
Frame Synchronization Code Structure

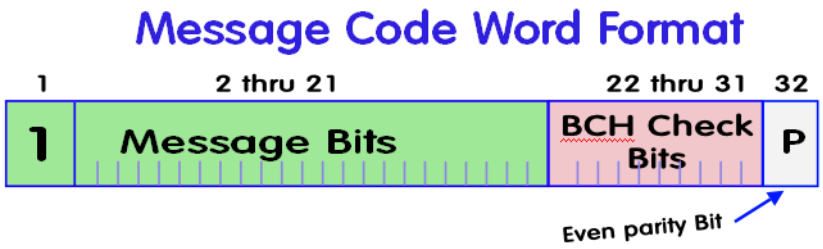
The frame synchronization code (FSC) is reserved word that is used to identify the beginning of each batch. The FS code word has 32 bits:

01111100110100100001010111011000

Code Words

Within a batch, there are two types of code words; an address code word and a message code word. Each contains 32 bits of information.





Address Code Word Structure

The structure of an address code word is shown above. The first bit of an address code work is always a 0. Bits 2 through 19 contain the address bits. The complete cap code is comprised of 18 address bits embedded in bits 2-19 and 3 bits derived from the frame location within the batch, for a total of 21 bits, for 2,097,152 unique cap codes.

Each POCSAG code word is capable of providing address information for four different paging “sources” (Source Address 1 through Source Address 4). These source addresses are determined by combinations of the values of the source identifier bits 20 and 21, sometimes called the Function Bits. Bits 22 through 31 are the BCH parity check bits, and bit 32 is the even parity bit.

The location of the frame within the batch is used to identify additional pager address bits. Pre-coded into the cap code are three bits which designate the frame location within the batch that the pager's address is received.

Most pagers and POCSAG receivers power down their receiver circuitry when during frames that are not intended for their specific cap code’s designated frame, which greatly extends pager battery life.

The two function bits are used to indicate the type of message that was sent. The standard convention for this bits is:

Bit 20	*Bit 21*	*Function*
0	0	
0	1	
1	0	

1	1	

Parity Check Bits

POCSAG uses a BCH Error Correcting Code (ECC) to detect and correct for bit errors. BCH provides a 6 bit hamming distance between all valid code words. With BCH, one or two bit errors can be corrected by the receiver. The BCH generating polynomial for (31,21) BCH code is $x^{10} + x^9 + x^8 + x^6 + x^5 + x^3 + 1$.

The BCH code used provides a 6 bit hamming distance between code words. This makes one or two bit error correction possible.

Optional Dual-Frame Operation

Two different frames can be selected on an ADVISOR pager. Each frame has two corresponding codes which provide a total of 16 addresses (sources) for POCSAG pagers. Selecting this option reduces battery life by about 30% in batch (synchronous) mode. The frame of codes A and B must be less than the frame of codes C and D. (The frame is the remainder of the address divided by 8).

Optional Alternate Frame Synchronization Code Words

The POCSAG standard reserved code words from 2,000,000 to 2,097,151. These reserved code words can be used to expand system capacity, as long as the paging system supports them. These reserved code words are called the Alternate Frame Synchronization (AFS) codes.

Code Capacity

The combination of the code plug's three pre-coded frame location bits and the address code word's 18 address bits provides over two million different assignable codes. In this combination, the frame location bits are the least-significant bits, and the ad dress bits are the most-significant bits.

Message Code Word Structure

A message sent to a pager consists of one address code word located in the proper frame within the batch and between 0 and n of the immediately following code words which contain the message text. The message ends when either an address code word is received or an idle code word is received. A long message may be spread over two or more 17 code word batches.

A message code word always starts with a 1 in bit 1 and always follows directly after the address. Each message code word replaces an address code word in the batch.

Idle Code Word Structure

The idle code word is a reserved code word used to fill a frame that does not have either a message code word or an address code word. If a frame contains only an address, such as when a tone-only pager is alerted, an idle code word completes the 64-bit frame. The idle code word comprises the 32 hex value of 0x7A89C197:

01111010100010011100000110010111

Numeric Messages

BCD numeric encoding packs 4 bit BCD symbols 5 to a message code word into bits 30-11.

The most significant nibble (bits 30,29,28,27) is the leftmost (or most significant) of a BCD coded message.

Values beyond 9 in each nibble (i.e. 0xA through 0xF) are encoded as follows:

- 0xA Reserved (possibly used for address extension)
- 0xB Character U (urgency)
- 0xC " ", Space (blank)
- 0xD "-", Hyphen (or dash)
- 0xE ")", Left bracket
- 0xF "(", Right bracket

BCD messages are space padded with trailing 0xC's to fill the code word.

POCSAG receivers output ASCII characters representing the numeric digits as shown in this table:

Numeric Digit	ASCII	ASCII Code		Numeric Digit	ASCII	ASCII Code
0x0	0	0x30		0x8	8	0x38
0x1	1	0x31		0x9	9	0x39
0x2	2	0x32		0xA	*	0x2A
0x3	3	0x33		0xB	U	0x55
0x4	4	0x34		0xC	*space*	0x20
0x5	5	0x35		0xD	-	0x2D
0x6	6	0x36		0xE	)	0x29
0x7	7	0x37		0xF	(	0x28

Alphanumeric Messages

Alphanumeric messages are comprised of a sequence of numbers and letters, using 7-bit ASCII characters. Characters are encoded in 7 bit ASCII format and assembled into the 20 bit message bits area of a message code word (bits 30-11). Three seven bit ASCII characters use 21 bits so if the message is 3 or more ASICC characters long, the first 20 bits of an ASCII message are in the first code word, the next 20 bits of a alphanumeric message are transmitted in the next code word, and so on. ASCII characters are placed from left to right (MSB to LSB). The LSb of an ASCII character is transmitted first.

The 7-bit ASCII code is used for alpha-numeric messages. There are 20 bits in each codeword for message data, however, in this format each character is 7 bits. Characters are split between codewords and the last codeword is filled with unprintable characters such as *end of message* , *end of text,* or *null*. Null is the only character which can be incomplete.

The maximum length for a standard alpha-numeric message is 40 characters. However, there are provisions for longer messages which allow up to 80 characters.

ASCII				b7	0	0	0	0	1	1	1	1
				b6	0	0	1	1	0	0	1	1
				b5	0	1	0	1	0	1	0	1
b4	b3	b2	b1		↓							
0	0	0	0	→	NUL	DLE	SP	0		P		p
0	0	0	1		SOH	DC	!	1	A	Q	a	q
0	0	1	0		STX	DC	"	2	B	R	b	r
0	0	1	1		ETX	DC	#	3	C	S	c	s
0	1	0	0		EOT	DC	$	4	D	T	d	t
0	1	0	1		ENQ	NAK	%	5	E	U	e	u
0	1	1	0		ACK	SYN	&	6	F		f	v
0	1	1	1		BEL	ETB	'	7	G	W	g	w
1	0	0	0		BS	CAN	(	8	H	X	h	x
1	0	0	1		HT	EM	)	9	I	Y	i	y
1	0	1	0		LF	SUB	*	:	J	Z	j	z
1	0	1	1		VT	ESC	+	;	K		k	
1	1	0	0		FF	FS	,	<	L		l	
1	1	0	1		CR	GS	-	=	M		m	
1	1	1	0		SO	RS	.	>	N	^	n	
1	1	1	1		SI	US	/	?	O	_	o	DEL

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