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Product Standards

Part No.	AN29160AA
Package Code No.	HSOP056-P-0300A

Analogue LSI Business Unit
Semiconductor Company
Matsushita Electric Industrial Co., Ltd.

Established by	Applied by	Checked by	Prepared by
T.Higuchi	M.Hiramatsu	T.Shimazu	K.Ohta

Established	Revised

Contents

AN29160AA

1chip IC for Transceiver (GMRS/ FRS/ PMR etc.)

■ Overview

AN29160AA is IC for Transceiver. One package involve four systems about IF, PLL, Regulator, and AF.
Involving 1st IFamp, 2nd Mixer, 2nd IFamp, FM-Detector, 460MHz PLL, Regulator for RXRF/ TXRF/ VCO/ MCU, OPAMPs for filter and Speaker Amplifier.
It is possible to reduce many external parts and space.

■ Features

(1) Operating Voltage : 6.5V ~ 3.2V
(2) Built in 1st IF Amplifier
(3) Built in 2nd Mixer
(4) Built in 2nd IF Amplifier
(5) Built in FM-Detector
(6) Built in PLL (Operating frequency :100 ~ 490MHz)
(7) Built in Regulator (ILmax=100mA)
(8) Built in 3Regulators (ILmax=20mA)
(9) Built in Speaker Amplifier (Pmax > 350mW @Vcc=4.5V/ RL=8ΩBTL)
(10) ElectricVolume control: 24 steps
(11) Built in 7 OPAMPs for Splatter-Filter, Data Filter, Voice Filter, Noise Filter, Microphone Amplifier.
(12) Built in RSSI , Noise Squlech.
(13) Built in VOX for Hands free comunication.
(14) Compact Package : HSOP56pin (0.5mm pitch)

■ Applications

- For Transceiver

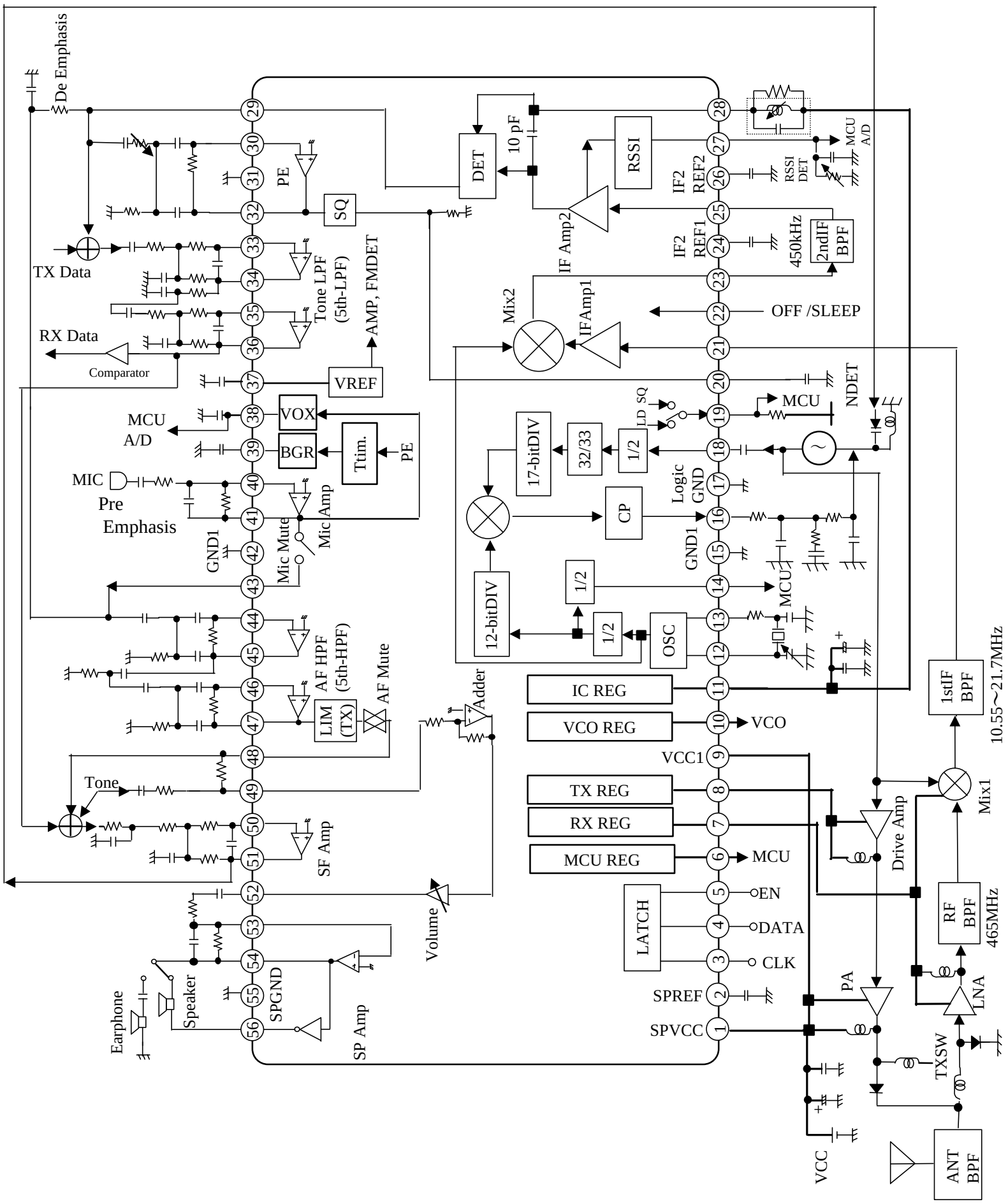
■ Package

- 56pin Plastic Small Outline Package With Heat Sink (SOP Type)

■ Type

- Silicon Monolithic BiCMOS IC

■ Application Circuit Example1



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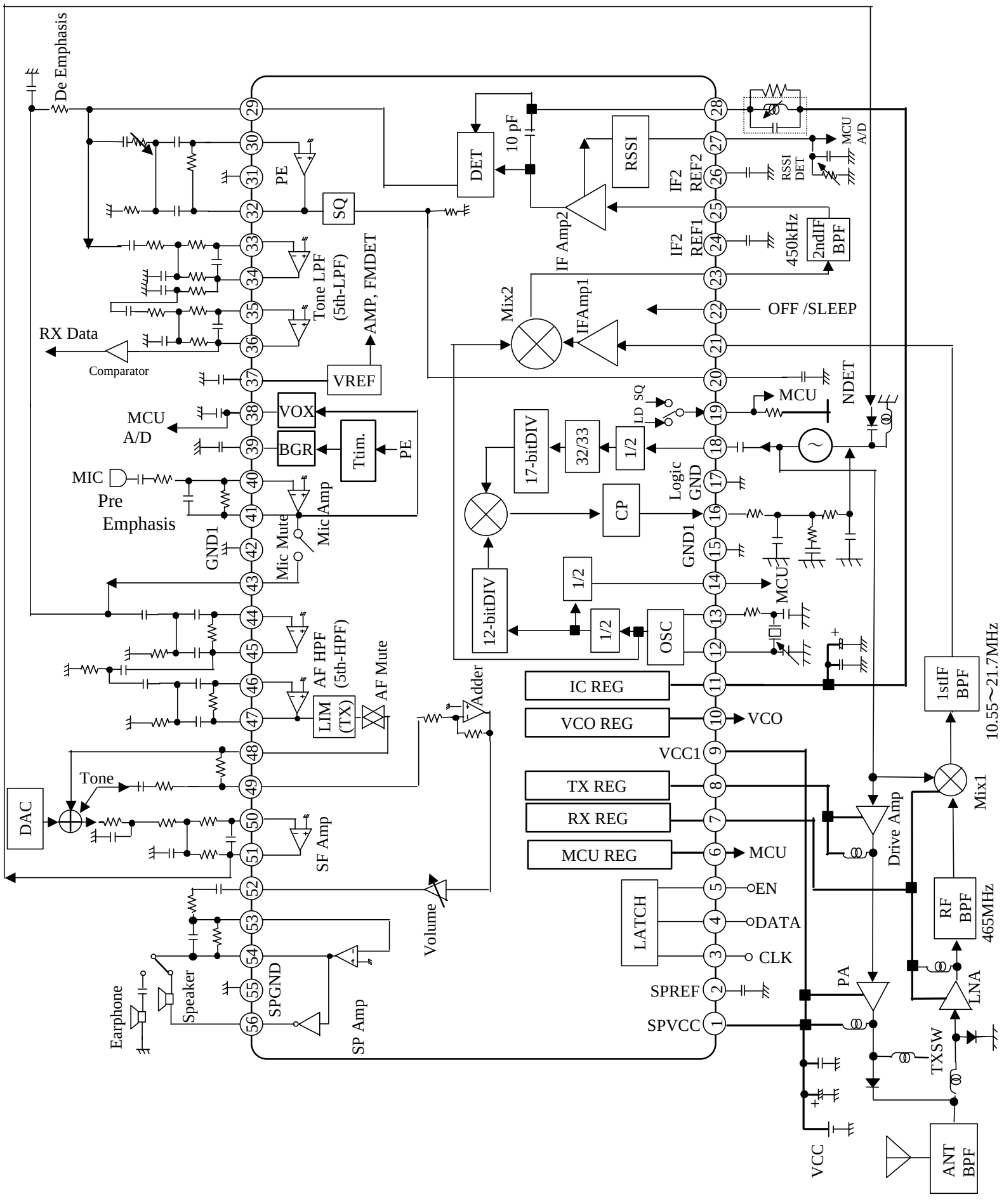
■ Application Circuit Example2



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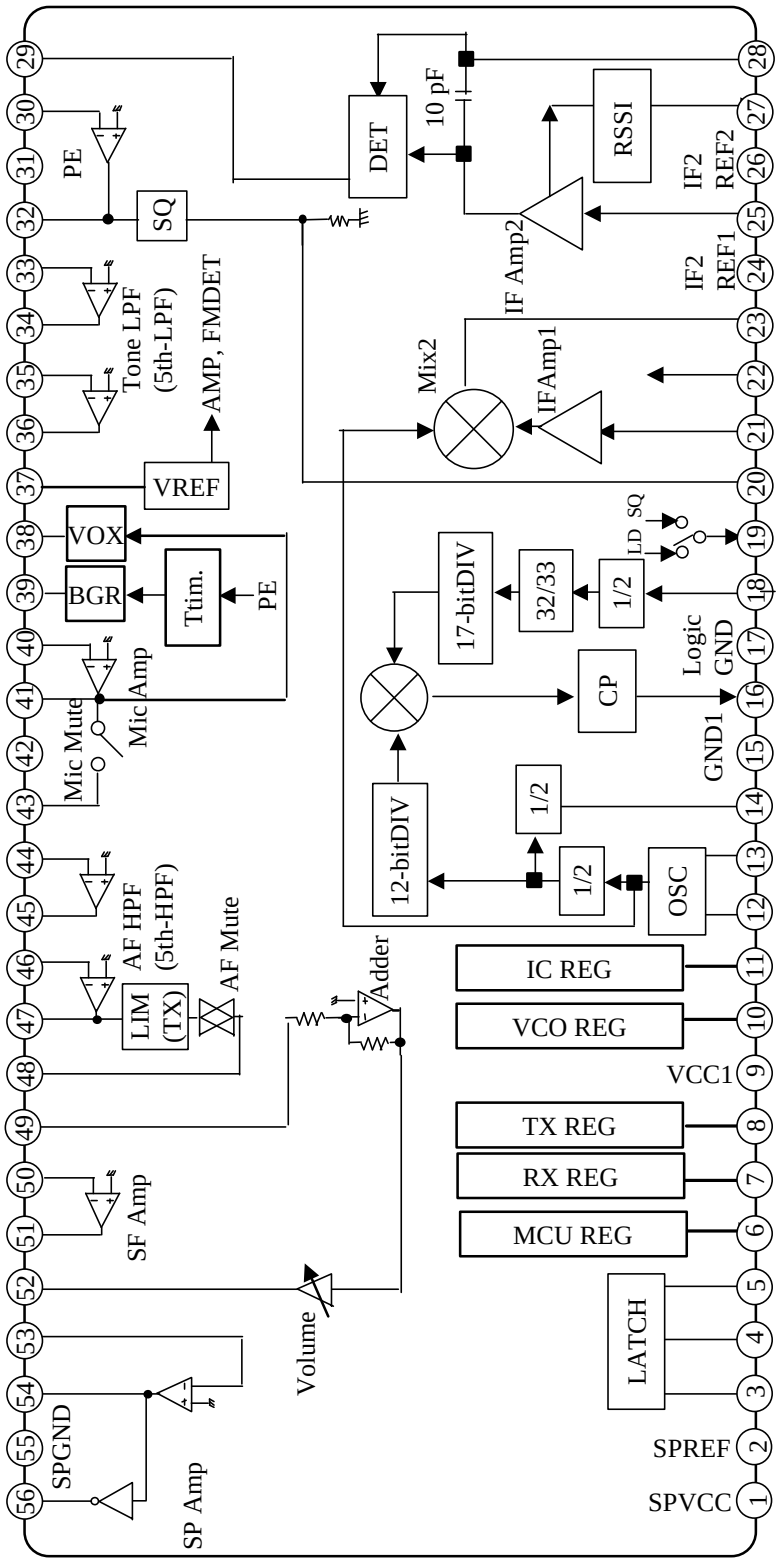
■ Block Diagram



■ Pin Descriptions

Pin No.	Pin name	Type	Description
1	SPVCC	I	Power Supply Pin for SP amp
2	SPREF	O	SP amp reference pin
3	CLKIN	I	Clock input pin
4	DATAIN	I	Serial data input Pin
5	ENIN	I	Enable input pin
6	MCUREG	O	Regulator output pin for MCU
7	RXREG	O	Regulator output pin for RX RF
8	TXREG	O	Regulator output pin for TX RF
9	VCC1	I	Power supply pin for Regulator/ Bias Circuit
10	VCOREG	O	Regulator output pin for VCO
11	ICREG	O	Regulator output pin for IC
12	OSCI	I	Oscillator input pin
13	OSCO	O	Oscillator output pin
14	OSCOUT	O	¼ Divider output
15	GND1	-	Ground
16	CP	O	Phase comparator output pin
17	VSS	-	Ground pin for Logic
18	PLLIN	I	PLL input pin
19	SIGOUT	O	LD,ND output pin
20	NDET	O	Noise detection
21	LIMIN	I	IF amp1 input pin
22	PCONT	I	Power Control pin
23	MIX2OUT	O	Mix2 output pin
24	IFREF1	O	Coupling pin for IF amp2 feedback
25	IFIN	I	IF amp2 input pin
26	IFREF2	O	Coupling pin for IF amp2 feedback
27	RSSIDET	O	RSSI rectification pin
28	TANK	O	IF amp2 output pin
29	DETOUT	O	FM Detector output pin
30	NFIN	I	NF amp input pin
31	PE	I	Zap current applied pin
32	NFOUT	O	NF amp output pin
33	LPF1IN	I	LPF1 input pin
34	LPF1OUT	O	LPF1 output pin
35	LPF2IN	I	LPF2 input pin

■ Pin Descriptions (continued)

Pin No.	Pin name	Type	Description
36	LPF2OUT	O	LPF2 output pin
37	BREF	O	Baseband Block Reference pin
38	VOXDET	O	VOX Detection pin
39	BGR	O	BGR reference pin
40	MICIN	I	Microphone amplifier input pin
41	MICOUT1	O	Microphone amplifier output pin
42	GND1	-	Ground
43	MICOUT2	O	Microphone amplifier mute output pin
44	HPF1IN	I	HPF1 input pin
45	HPF1OUT	O	HPF1 output pin
46	HPF2IN	I	HPF2 input pin
47	HPF2OUT	O	HPF2 output pin,Limiter input pin
48	AMOUT	O	AF mute output pin
49	TONE	I	Adder input pin
50	SFIN	I	SF amp input pin
51	SFOUT	O	SF amp output pin
52	EVOUT	O	Electric Volume output pin
53	SPIN	I	SP amp input pin
54	SPOUT1	O	SP amp output pin
55	SPGND	-	Ground pin for SP amp
56	SPOUT2	O	SP amp output pin

■ Absolute Maximum Ratings

A No.	Parameter	Symbol	Rating	Unit	Note
1	Supply voltage	V_{CC1}	6.7	V	*1
		SPV_{CC}	6.7		
2	Supply current	I_{CC}	-	A	-
3	Power dissipation	P_D	517	mW	*2
4	Operating ambient temperature	T_{opr}	-30 to +75	°C	*3
5	Storage temperature	T_{stg}	-55 to +150	°C	*3

Notes) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: The power dissipation shown is the value at T_a = 75°C for the independent (unmounted) IC package without a heat sink.
When using this IC, refer to the P_D-T_a diagram of the package standard page 4 and use under the condition not exceeding the allowable value.

*3: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

■ Operating supply voltage range

Parameter	Symbol	Range	Unit	Note
Operating supply voltage range	V_{CC1}	3.2 to 6.5	V	*
	SPV_{CC}	3.2 to 6.5		*

Note) *:The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

■ Allowed Voltage Ranges

Note) • The ranges on the list are the voltages of respective pins in relation to GND.
The GND represents the voltage of GND1,VSS and SPGND. And GND1=VSS=SPGND.
• Do not apply the voltages or the currents from external into the pins which are not on the list.

Pin No.	Pin name	Range	Unit	Note
1	SPVCC	0 to 6.5	V	—
3	CLKIN	0 to ICREG	V	—
4	DATAIN	0 to ICREG	V	—
5	ENIN	0 to ICREG	V	—
6	MCUREG	0 to -20	mA	—
7	RXREG	0 to -20	mA	—
8	TXREG	0 to -100	mA	—
9	VCC1	0 to 6.5	V	—
10	VCOREG	0 to -20	mA	—
11	ICREG	0 to -3	mA	—
12	OSCI	0 to ICREG	V	—
18	PLLIN	0 to ICREG	V	—
21	LIMIN	0 to ICREG	V	—
22	PCONT	0 to VCC1	V	—
25	IFIN	0 to ICREG	V	—
30	NFIN	0 to ICREG	V	—
31	PE	0	V	—
33	LPF1IN	0 to ICREG	V	—
35	LPF2IN	0 to ICREG	V	—
40	MICIN	0 to ICREG	V	—
44	HPF1IN	0 to ICREG	V	—
46	HPF2IN	0 to ICREG	V	—
49	TONE	0 to ICREG	V	—
50	SFIN	0 to ICREG	V	—
53	SPIN	0 to SPVCC	V	—

Pin No.	Pin name	Range	Unit	Note

■ Electrical Characteristics at V_{CC} = 4.5V

Note) T_a = 25°C±2°C, fin = 1kHz unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Notes
					Min	Typ	Max		
< Total >									
1	Current Drain in RX Mode	IRX	1	PLL/ IF/ RXAF/ RXREG/ VCOREG: Active	-	21	27.3	mA	
2	Current Drain in STBY Mode	IST	1	PLL/ IF/RXREG/ VCOREG: Active	-	12.3	16	mA	
3	Current Drain in TX Mode	ITX	1	PLL/ TXAF/ TXREG/ VCOREG: Active	-	10.4	13.5	mA	
4	Current Drain in Call Tone Mode	ICT	1	PLL/ RXAF/ TXAF/ TXREG/ VCOREG: Active	-	16.8	21.8	mA	
5	Current Drain in Sleep Mode	ISL	1	XO/ 1/4Div/ MCUREG/ ICREG: Active	-	1.8	2.4	mA	
6	Current Drain in Cutoff Mode	ICUT	1	V22=L	-	6	10	uA	
< DC POWER SUPPLY >									
7	IC REG Output Voltage	VIC	1	No Load	2.71	2.8	2.89	V	
8	MCU REG Output Voltage in Active Mode	VMCU	1	V22=H, No Load	2.71	2.8	2.89	V	
9	MCU REG Output Voltage in Cutoff Mode	VMCU2	1	V22=L, No Load	2	2.35	2.7	V	
10	VCO REG Output Voltage (3cell mode)	VVCO3	1	No Load	2.81	2.9	2.99	V	
11	VCO REG Output Voltage (4cell mode)	VVCO4	1	VCC=6V No Load	3.68	4	4.32	V	
12	RX REG Output Voltage (3cell mode)	VRX3	1	No Load	2.71	2.8	2.89	V	
13	RX REG Output Voltage (4cell mode)	VRX4	1	VCC=6V No Load	3.68	4	4.32	V	
14	TX REG Output Voltage (3cell mode)	VTX3	1	No Load	2.71	2.8	2.89	V	
15	TX REG Output Voltage (4cell mode)	VTX4	1	VCC=6V No Load	3.68	4	4.32	V	
< IFamp2 + FM DET>									
16	FM Detection Output Level	VDET	1	fin= 450kHz, fm= 1kHz, Δf= ±1.5kHz	-19.5	-16.5	-13.5	dBV	
17	Distortion	DDET	1	fin= 450kHz, fm= 1kHz, Δf= ±1.5kHz	-	1.5	3	%	

■ Electrical Characteristics at V_{CC} = 4.5V

Note) T_a = 25°C±2°C, fin = 1kHz unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Notes
					Min	Typ	Max		
< DeEmp + AF HPF + EVOL + Sp amp >									
18	Standard Output Level	VORX	1	Vin44 = -15dBV RL = 8Ω	-3	0	3	dBV	*1
19	Distortion	DORX	1	Vin44 = -15dBV RL = 8Ω	-	1.5	3	%	*1
< Mic Amp + AFHPF + SF Amp >									
20	Standard Output Level	VOTX	1	Vin40 = -45dBV RL = 10kΩ	-12	-9	-6	dBV	
21	Distortion	DOTX	1	Vin40 = -45dBV RL = 10kΩ	-	0.5	2	%	

Note)*1: Electric Volume: -8dB Mode

■Electrical Characteristics (Reference values for design) at VCC = 4.5V, 6.0V

Notes) 1. Ta = 25°C±2°C, fin = 1kHz unless otherwise specified.
2. The following values are design reference values. These values do not guarantee the characteristics of the device. Furthermore, they do not guarantee that all devices are tested.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference values			Unit	Notes
					Min	Typ	Max		
< DC POWER SUPPLY >									
1	IC REG Output Current	ILIC	1	0.1V Drop from No Load	1	-	-	mA	*1
2	MCU REG Output Current in Active Mode	ILMCU	1	0.1V Drop from No Load V22=H	20	-	-	mA	*1
3	MCU REG Output Current in Cutoff Mode	ILMCU2	1	0.1V Drop from No Load V22=L	100	-	-	uA	*1
4	VCO REG Output Current (3cell)	ILVCO3	1	0.1V Drop from No Load	20	-	-	mA	*1
5	VCO REG Output Current (4cell)	ILVCO4	1	0.1V Drop from No Load	20	-	-	mA	*1
6	RX REG Output Current (3cell)	ILRX3	1	0.1V Drop from No Load	20	-	-	mA	*1
7	RX REG Output Current (4cell)	ILRX4	1	0.1V Drop from No Load	20	-	-	mA	*1
8	TX REG Output Current (3cell)	ILTX3	1	0.1V Drop from No Load	100	-	-	mA	*1
9	TX REG Output Current (4cell)	ILTX4	1	0.1V Drop from No Load	100	-	-	mA	*1
10	IC REG Ripple Rejection Ratio	RRIC	1	Vin = 1kHz, 0.1Vpp RX Mode, IL = 1mA	-	-60	-	dB	*1
11	MCU REG Ripple Rejection Ratio	RRMCU	1	Vin = 1kHz, 0.1Vpp Active Mode, IL = 20mA	-	-60	-	dB	*1
12	VCO REG (3cell) Ripple Rejection Ratio	RRVCO3	1	Vin = 1kHz, 0.1Vpp RX Mode, IL = 20mA	-	-60	-	dB	*1
13	VCO REG (4cell) Ripple Rejection Ratio	RRVCO4	1	Vin = 1kHz, 0.1Vpp RX Mode, IL = 20mA	-	-60	-	dB	*1
14	RX REG (3cell) Ripple Rejection Ratio	RRRX3	1	Vin = 1kHz, 0.1Vpp RX Mode, IL = 20mA	-	-60	-	dB	*1
15	RX REG (4cell) Ripple Rejection Ratio	RRRX4	1	Vin = 1kHz, 0.1Vpp RX Mode, IL = 20mA	-	-60	-	dB	*1
16	TX REG (3cell) Ripple Rejection Ratio	RRTX3	1	Vin = 1kHz, 0.1Vpp TX Mode, IL = 100mA	-	-60	-	dB	*1
17	TX REG (4cell) Ripple Rejection Ratio	RRTX4	1	Vin = 1kHz, 0.1Vpp TX Mode, IL = 100mA	-	-60	-	dB	*1

Note) *1: The above characteristics are logical values derived from the design of the IC and are not guaranteed by inspection. If a problem does occur related to these characteristics, Matsushita will respond in good faith to user concerns.

■Electrical Characteristics (Reference values for design) at V_{CC} = 6.0V

Notes) 1. T_a = 25°C±2°C, fin = 1kHz unless otherwise specified.
2. The following values are design reference values. These values do not guarantee the characteristics of the device. Furthermore, they do not guarantee that all devices are tested.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference values			Unit	Notes
					Min	Typ	Max		
< Total >									
18	Current Drain in RX Mode	IRX	1	PLL/ IF/ RXAF/ RXREG/ VCOREG: Active	-	21	35.5	mA	*1
19	Current Drain in STBY Mode	IST	1	PLL/ IF/RXREG/ VCOREG: Active	-	13	20.8	mA	*1
20	Current Drain in TX Mode	ITX	1	PLL/ TXAF/ TXREG/ VCOREG: Active	-	11	17.6	mA	*1
21	Current Drain in Call Tone Mode	ICT	1	PLL/ RXAF/ TXAF/ TXREG/ VCOREG: Active	-	17	28.3	mA	*1
22	Current Drain in Sleep Mode	ISL	1	XO/ 1/4Div/ MCUREG/ ICREG: Active	-	2	3.1	mA	*1
23	Current Drain in Cutoff Mode	ICUT	1	V22=L	-	8	16	uA	*1
< DC POWER SUPPLY >									
24	IC REG Output Voltage	VIC	1	No Load	2.63	2.8	2.98	V	*1
25	MCU REG Output Voltage in Active Mode	VMCU	1	V22=H, No Load	2.63	2.8	2.98	V	*1
26	MCU REG Output Voltage in Cutoff Mode	VMCU2	1	V22=L, No Load	2	2.4	3	V	*1
27	VCO REG Output Voltage (3cell mode)	VVCO3	1	No Load	2.73	2.9	3.08	V	*1
28	VCO REG Output Voltage (4cell mode)	VVCO4	1	VCC=4.5V No Load	3.57	4	4.45	V	*1
29	RX REG Output Voltage (3cell mode)	VRX3	1	No Load	2.63	2.8	2.98	V	*1
30	RX REG Output Voltage (4cell mode)	VRX4	1	VCC=4.5V No Load	3.57	4	4.45	V	*1
31	TX REG Output Voltage (3cell mode)	VTX3	1	No Load	2.63	2.8	2.98	V	*1
32	TX REG Output Voltage (4cell mode)	VTX4	1	VCC=4.5V No Load	3.57	4	4.45	V	*1
< IFamp2 + FM DET>									
33	FM Detection Output Level	VDET	1	fin= 450kHz, fm= 1kHz, Δf= ±1.5kHz	-20	-16.5	-13	dBV	*1
34	Distortion	DDET	1	fin= 450kHz, fm= 1kHz, Δf= ±1.5kHz	-	1.5	3	%	*1

Note) *1: The above characteristics are logical values derived from the design of the IC and are not guaranteed by inspection. If a problem does occur related to these characteristics, Matsushita will respond in good faith to user concerns.

■Electrical Characteristics (Reference values for design) at V_{CC} = 6.0V

Notes) 1. T_a = 25°C±2°C, fin = 1kHz unless otherwise specified.

2. The following values are design reference values. These values do not guarantee the characteristics of the device. Furthermore, they do not guarantee that all devices are tested.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference values			Unit	Notes
					Min	Typ	Max		
< DeEmp + AF HPF + EVOL + Sp amp >									
35	Standerd Output Level	VORX	1	Vin44 = -15dBV RL = 8Ω	-3.5	0	3.5	dBV	*1,2
36	Distortion	DORX	1	Vin44 = -15dBV RL = 8Ω	-	1.5	3	%	*1,2
< Mic Amp + AFHPF + SF Amp >									
37	Standerd Output Level	VOTX	1	Vin40 = -45dBV RL = 10kΩ	-12.5	-9	-5.5	dBV	*1
38	Distortion	DOTX	1	Vin40 = -45dBV RL = 10kΩ	-	0.5	2	%	*1

Note) *1: The above characteristics are logical values derived from the design of the IC and are not guaranteed by inspection. If a problem does occur related to these characteristics, Matsushita will respond in good faith to user concerns.

Note)*2: Electric Volume: -8dB Mode

■Electrical Characteristics (Reference values for design) at VCC = 4.5V, 6.0V

Notes) 1. Ta = 25°C±2°C, fin = 1kHz unless otherwise specified.
2. The following values are design reference values. These values do not guarantee the characteristics of the device. Furthermore, they do not guarantee that all devices are tested.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference values			Unit	Notes
					Min	Typ	Max		
IF Section < IFamp1 + MIX2 >									
39	Gain	GMX	1	fIF1= 21.7MHz fLO= 21.25MHz	-	36	-	dB	*1
40	1dB Compression Input Level	V1dB	-	fIF1= 21.7MHz fLO= 21.25MHz	-	-36	-	dBm	*1
41	3rd Intercept Point Input Level	IP3	-	fIF1= 21.65MHz+ 21.6MHz fLO= 21.25MHz	-	-26	-	dBm	*1
42	Input Resistance	ZMXIR	-	fIF1= 21.7MHz	-	670	-	Ω	*1
43	Input Capacitance	ZMXIC	-	fIF1= 21.7MHz	-	4.9	-	pF	*1
44	Output Resistance	ZMXOR	-	fIF2= 450kHz	-	1.5	-	kΩ	*1
< IFamp2 + FMDET >									
45	Input Resistance	ZIF2IR	-	fIF2= 450kHz	-	1.5	-	kΩ	*1
46	Gain	GIF2	-	fIF2= 450kHz	-	70	-	dB	*1
47	-3dB Limiting Sensitivity	LIF2	-	fIF2= 450kHz	-	-75	-	dBm	*1
48	FM Detection Output S/N Ratio	VDETSN	1	fin= 450kHz, fm= 1kHz, Δf= ±1.5kHz/ 0kHz	43	50	-	dB	*1
< IFamp1 + MIX2 + IFamp2 + FMDET >									
49	12dB SINAD Sensitivity1	SENS1	-	fIF1= 21.7MHz Input 50Ω terminated with CCITT-TEL53 Filter	-	-103	-	dBm	*1
50	12dB SINAD Sensitivity2	SENS2	-	fIF1= 21.7MHz Input 50Ω terminated with 30kHz LPF	-	-94	-	dBm	*1
< IFamp1 + MIX2 + IFamp2 + RSSI >									
51	Input Dynamic Range	DIRS	-		-	50	-	dB	*1
52	Max Output Voltage	VHRS	1	Vin21 = 21.7MHz, -20dBm	1.8	2.2	-	V	*1
53	Min Output Voltage	VLRS	1	Vin21 = OFF	-	0.1	1.0	V	*1
< Noise Filter + SQ >									
54	Threshold Level	THNQ	1	Voltage on pin20 when pin 19 is set to high level from low level	-	0.77	-	V	*1
55	Squelch Hysteresis	HYNQ	1	Difference in voltage between pin 20 and THNQ when pin 19 is set to low level from high level	-	55	-	mV	*1

Note) *1: The above characteristics are logical values derived from the design of the IC and are not guaranteed by inspection. If a problem does occur related to these characteristics, Matsushita will respond in good faith to user concerns.

■Electrical Characteristics (Reference values for design) at VCC = 4.5V, 6.0V

Notes) 1. Ta = 25°C±2°C, fin = 1kHz unless otherwise specified.
2. The following values are design reference values. These values do not guarantee the characteristics of the device. Furthermore, they do not guarantee that all devices are tested.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference values			Unit	Notes
					Min	Typ	Max		
LOGIC SECTION < SIGOUT >									
56	Low Level Output Voltage	LSIG	1	in high electric field or with PLL locked RL=100kΩ	-	0.2	0.4	V	*1
57	High Level Output Voltage	HSIG	1	in low electric field or with PLL unlocked RL=100kΩ	MCUREG x0.8	MCUREG	MCUREG	V	*1
< Serial Data Decorder >									
58	Low Level Input Voltage	LSC	-		0	-	0.2	V	*1
59	High Level Input Voltage	HSC	-		IC REG x 0.7	-	IC REG	V	*1
60	Input Clock Frequency	FSC	-		-	-	1	MHz	*1
< Cut OFF mode setting >									
61	Low Level Input Voltage	LPC	1	Cutoff setting	0	-	0.4	V	*1
62	High Level Input Voltage	HPC	1	Active setting	1.3	-	VCC	V	*1

Note) *1: The above characteristics are logical values derived from the design of the IC and are not guaranteed by inspection. If a problem does occur related to these characteristics, Matsushita will respond in good faith to user concerns.

■Electrical Characteristics (Reference values for design) at VCC = 4.5V, 6.0V

Notes) 1. Ta = 25°C±2°C, fin = 1kHz unless otherwise specified.
2. The following values are design reference values. These values do not guarantee the characteristics of the device. Furthermore, they do not guarantee that all devices are tested.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference Values			Unit	Notes
					Min	Typ	Max		
RX Voice System < Adder + Electrical Volume >									
63	Standard Output Level	VEV	1	Vin49 = 0dBV -8dB Mode	-	-17	-	dBV	*1
64	Output Dynamic Range	DOEV	1	THD=5% RL=10kΩ 0dB Mode	-3	-	-	dBV	*1
65	Input Dynamic Range	DIEV	1	AC Level on pin49 @ THD=5%, All Mode	-	-16	-	dBV	*1
66	Volume Control Attenuation	AEV	1	Step 1 to 23	40	44	48	dB	*1
67	Volume Mute Attenuation	MEV	1	Vin49 = 0dBV Mute Mode	-	-57	-	dB	*1
< SPAmp >									
68	Max Output Power 1	PSP1	1	Vcc=4.5V, BTL Output THD= 10%, RL=8Ω	350	500	-	mW	*1
69	Max Output Power 2	PSP2	-	Vcc=4.5V, BTL Output THD= 10%, RL=16Ω	200	300	-	mW	*1
70	Max Output Power 3	PSP3	1	Vcc=6V, Single Output THD= 10%, RL=8Ω	250	350	-	mW	*1
71	Max Output Power 4	PSP4	-	Vcc=6V, Single Output THD= 10%, RL=16Ω	140	200	-	mW	*1
72	Max Output Power 5	PSP5	-	Vcc=4.5V, Single Output THD= 10%, RL=8Ω	130	190	-	mW	*1
73	Max Output Power 6	PSP6	-	Vcc=4.5V, Single Output THD= 10%, RL=16Ω	70	100	-	mW	*1
< DeEmp + AFHPF + EVOL + SPAmp >									
74	Output Dynamic Range VCC=4.5V	DORX1	1	THD=10%, RL=8Ω	2.5	5	-	dBV	*1
75	Output Dynamic Range VCC=6.0V	DORX2	1	THD=10%, RL=8Ω	-	9	-	dBV	*1
76	Output Noise Level	NRX	1	30kHz LPF	-	-53	-45	dBV	*1
77	Mute Attenuation	MRX	1	Vin44 = -15dBV AFMute/ EVMute: Active	-	-65	-	dB	*1
RX Data System < IFAMP2 + FMDET + DataLPF>									
78	Standard Output Level	VDR	1	fin= 450kHz, fm= 160Hz, Δf= ±0.5kHz	-	-7	-	dBV	*1

Note) *1: The above characteristics are logical values derived from the design of the IC and are not guaranteed by inspection. If a problem does occur related to these characteristics, Matsushita will respond in good faith to user concerns.

■Electrical Characteristics (Reference values for design) at VCC = 4.5V, 6.0V

Notes) 1. Ta = 25°C±2°C, fin = 1kHz unless otherwise specified.
2. The following values are design reference values. These values do not guarantee the characteristics of the device. Furthermore, they do not guarantee that all devices are tested.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference Values			Unit	Notes
					Min	Typ	Max		
TX Voice System < MICAMP >									
79	Mute Attenuation	MMIC	1	Vin40 = -45dBV	-	-60	-	dB	*1
< MICAMP + LIM >									
80	Limit Level	LIM	1	VIn40 = -30dBV	-	-10	-	dBV	*1
< MICAMP + LIM + SFAMP >									
81	Output Noise Level	NRX	1	30kHz LPF	-	-65	-55	dBV	*1
82	Mute Attenuation	MRX	1	Vin40 = -45dBV AFMute/ MICMute: Active	-	-65	-	dB	*1
< MICAMP + VOX >									
83	Max Output Voltage	VHVOX	1	Vin40 = -10dBV	1.8	2.2	-	V	*1
84	Min Output Voltage	VLVOX	1	Vin40 = OFF	-	-	0.08	V	*1
85	Output Voltage Difference between RX/TX Mode	DVOX	1	Vin40= OFF	0	-	30	mV	*1
TXData System <DataLPF + SFAmp >									
86	Standard Output Level	VDT	1	Vin33 = 160Hz, 0dBV RL = 10kΩ	-	-18.5	-	dBV	*1
Tone System <Adder + EVOL + SPAmp >									
87	Standard Output Level	VTR	1	Vin49 = 0dBV -8dB Mode	-	0	-	dBV	*1
88	Output Dynamic Range VCC=4.5V	DOTR1	1	THD=10% RL= 8Ω -8dB Mode	-	5	-	dBV	*1
89	Output Dynamic Range VCC=6V	DOTR2	1	THD=10% RL= 8Ω -8dB Mode	-	9	-	dBV	*1
90	Output Noise Level	NTR	1	30kHz LPF	-	-65	-55	dBV	*1
< SFAmp >									
91	Standard Output Level	VTR	1	Vin49 = 0dBV RL = 10kΩ	-	-8.5	-	dBV	*1
92	Output Dynamic Range	DORX	1	THD=5%, RL=10kΩ	-3	-1	-	dBV	*1
93	Output Noise Level	NRX	1	30kHz LPF	-	-65	-55	dBV	*1
94	Mute Attenuation	MRX	1	Vin49=0dBV SFMute: Active	-	-60	-	dB	*1

Note) *1: The above characteristics are logical values derived from the design of the IC and are not guaranteed by inspection. If a problem does occur related to these characteristics, Matsushita will respond in good faith to user concerns.

■Electrical Characteristics (Reference values for design) at VCC = 4.5V, 6.0V

Notes) 1. Ta = 25°C±2°C, fin = 1kHz unless otherwise specified.
2. The following values are design reference values. These values do not guarantee the characteristics of the device. Furthermore, they do not guarantee that all devices are tested.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference values			Unit	Notes
					Min	Typ	Max		
PLL SECTION < Charge Pump >									
95	Low Level Output Voltage 1mA mode	CPVL1	1	No load	-	-	0.15	V	*1
96	Low Level Output Voltage 100uA mode	CPVL2	1	No load	-	-	0.15	V	*1
97	High Level Output Voltage 1mA mode	CPVH1	1	No load	2.4	-	-	V	*1
98	High Level Output Voltage 100uA mode	CPVH2	1	No load	2.4	-	-	V	*1
99	Nch Output Current 800uA mode	CPN1	1	V16 = 1.4V	400	800	1600	uA	*1
100	Nch Output Current 100uA mode	CPN2	1	V16 = 1.4V	50	100	200	uA	*1
101	Pch Output Current 800uA mode	CPP1	1	V16 = 1.4V	-1600	-800	-400	uA	*1
102	Pch Output Current 100uA mode	CPP2	1	V16 = 1.4V	-200	-100	-50	uA	*1
103	Output Leakage Current	ILE	-		-100	0	100	nA	*1
< PLL Counter >									
104	Input Sensitivity	VCND	1	Input 50Ω terminated	-20	-	0	dBm	*1
105	Operating Frequency	FCN	1	Input 50Ω terminated	100	-	490	MHz	*1
< X'tal Oscillator >									
106	Oscillation Margin1	RM1	-	f = 10.1MHz CL=16pF Ro= 100Ω	400	800	-	Ω	*1
107	Oscillation Margin2	RM2	-	f = 21.25MHz CL=10pF Ro= 100Ω	200	400	-	Ω	*1
< 4divider Output >									
108	Output Level	VXO4	1	fo= 5.3MHz, RL= 10kΩ	-	-10	-	dBm	*1
< IFamp1 + MIX2 >									
109	Spurious 1	SPR1	-	fIF1=32.325MHz -35dBm fLO=21.25MHz	-	-70	-	dBm	*1
110	Spurious 2	SPR2	-	fIF1=11.075MHz -35dBm fLO=21.25MHz	-	-62	-	dBm	*1
111	Spurious 3	SPR3	-	fIF1=15.6MHz -35dBm fLO=10.1MHz	-	-66	-	dBm	*1
112	Spurious 4	SPR4	-	fIF1=5.5MHz -35dBm fLO=10.1MHz	-	-69	-	dBm	*1

Note) *1: The above characteristics are logical values derived from the design of the IC and are not guaranteed by inspection. If a problem does occur related to these characteristics, Matsushita will respond in good faith to user concerns.

■ Control Pin Mode Table

Note) See parameters 61 to 62 in the Electrical Characteristics for control voltage retention ranges.

Pin No.	Description	Pin voltage		Remarks
		Low	High	
22	Power Control	Cut Off	Active	-

■ Test Circuit Diagram1

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■ Electrical Characteristics Test Procedures

C No.	Parameter	Input		Output		Pin settings								
		Pin No.	Conditions	Pin No.	Conditions	V22	SW 23	SW 40	SW 44	SW 44A	SW 44B	SW 49	SW 53A	
<Total>														
1	Current Drain in RX Mode	VCC	4.5V	ICC		1.2V	a	a	OFF	OFF	ON	a	OFF	
2	Current Drain in STBY Mode	VCC	4.5V	ICC		1.2V	a	a	OFF	OFF	ON	a	OFF	
3	Current Drain in TX Mode	VCC	4.5V	ICC		1.2V	a	a	OFF	OFF	ON	a	OFF	
4	Current Drain in Call Tone Mode	VCC	4.5V	ICC		1.2V	a	a	OFF	OFF	ON	a	OFF	
5	Current Drain in Sleep Mode	VCC	4.5V	ICC		1.2V	a	a	OFF	OFF	ON	a	OFF	
6	Current Drain in Cutoff Mode	VCC	4.5V	ICC		0.5V	a	a	OFF	OFF	ON	a	OFF	
<DC POWER SUPPLY>														
7	IC REG Output Voltage	VCC	4.5V	VM11	No Load	1.2V	a	a	OFF	OFF	ON	a	OFF	
8	MCU REG Output Voltage in Active Mode	VCC	4.5V	VM6	No Load	1.2V	a	a	OFF	OFF	ON	a	OFF	
9	MCU REG Output Voltage in Cutoff Mode	VCC	4.5V	VM6	No Load	0.5V	a	a	OFF	OFF	ON	a	OFF	
10	VCO REG Output Voltage (3cell mode)	VCC	4.5V	VM10	No Load	1.2V	a	a	OFF	OFF	ON	a	OFF	
11	VCO REG Output Voltage (4cell mode)	VCC	6.0V	VM10	No Load	1.2V	a	a	OFF	OFF	ON	a	OFF	
12	RX REG Output Voltage (3cell mode)	VCC	4.5V	VM7	No Load	1.2V	a	a	OFF	OFF	ON	a	OFF	
13	RX REG Output Voltage (4cell mode)	VCC	6.0V	VM7	No Load	1.2V	a	a	OFF	OFF	ON	a	OFF	
14	TX REG Output Voltage (3cell mode)	VCC	4.5V	VM8	No Load	1.2V	a	a	OFF	OFF	ON	a	OFF	
15	TX REG Output Voltage (4cell mode)	VCC	6.0V	VM8	No Load	1.2V	a	a	OFF	OFF	ON	a	OFF	

SW3=a SW4=a SW5=a SW10=OFF SW16=OFF SW16B=OFF SW18=a SW30=OFF
SW31=a SW33=a SW53=OFF SW54=ON SW54A=OFF

■ Electrical Characteristics Test Procedures

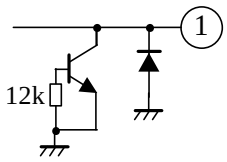
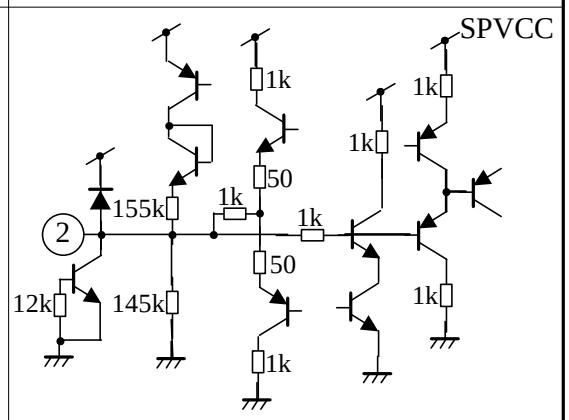
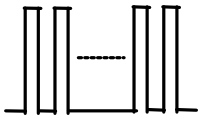
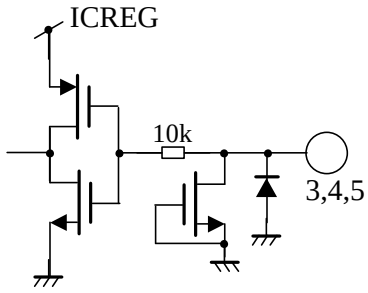
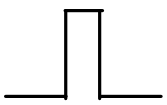
C No.	Parameter	Input		Output		Pin settings								
		Pin No.	Conditions	Pin No.	Conditions	V22	SW 23	SW 40	SW 44	SW 44A	SW 44B	SW 49	SW 53A	
<IFAMP2 + FMDET>														
16	FM Detection Output Level	VIN23	fin= 450kHz, fm= 1kHz, Δf=±1.5kHz,0dBm	VM29		1.2V	b	a	OFF	ON	OFF	a	OFF	
17	Distortion	VIN23	fin= 450kHz, fm= 1kHz, Δf= ±1.5kHz,0dBm	VM29		1.2V	b	a	OFF	ON	OFF	a	OFF	
<DeEmp + AF HPF + EVOL + SpAmp>														
18	Standerd Output Level	VIN44	Vin = 1kHz,-15dBV	VM56	RL = 8Ω	1.2V	a	a	ON	OFF	OFF	a	ON	
19	Distortion	VIN44	Vin = 1kHz,-15dBV	VM56	RL = 8Ω	1.2V	a	a	ON	OFF	OFF	a	ON	
<MicAmp + AF HPF + SF Amp>														
20	Standerd Output Level	VIN40	Vin = 1kHz,-45dBV	VM51	RL = 10kΩ	1.2V	a	b	OFF	ON	OFF	a	OFF	
21	Distortion	VIN40	Vin = 1kHz,-45dBV	VM51	RL = 10kΩ	1.2V	a	b	OFF	ON	OFF	a	OFF	

SW3=a SW4=a SW5=a SW10=OFF SW16=OFF SW16B=OFF SW18=a SW30=OFF
SW31=a SW33=a SW53=OFF SW54=ON SW54A=OFF

■ Technical Data

1.I/O block circuit diagrams and pin function descriptions

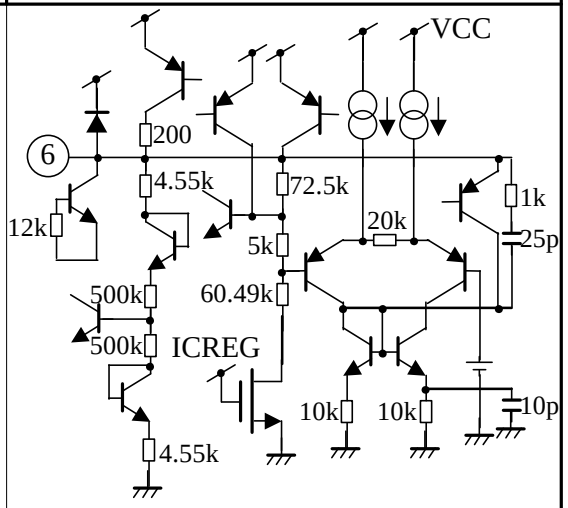
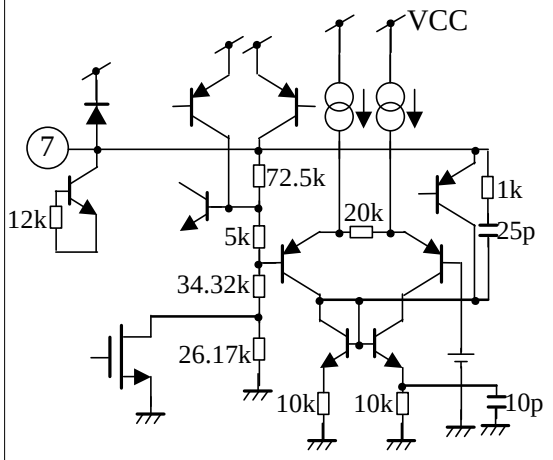
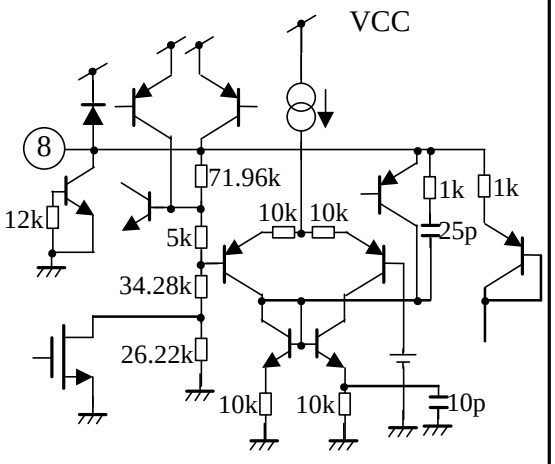
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Pin Name	Waveform and voltage	Function	Inner circuit
1	SPVCC	DC	DC Power Supply Pin for SPAMP	
2	SPREF	DC	SPAMP reference pin	
3	CLKIN		Clock input pin Pin for sync clock input in order to read serial data	
4	DATAIN		Serial data input Pin This pin is used by the internal shift register to read serial data at the rising edge of the clock	
5	ENIN		Enable input pin Serial data is deemed to be completed at the rising edge of the signal and the serial data is read by each latch circuit according to the settings in D1,D2,D3 and D4	

■ Technical Data

1.I/O block circuit diagrams and pin function descriptions (Continued)

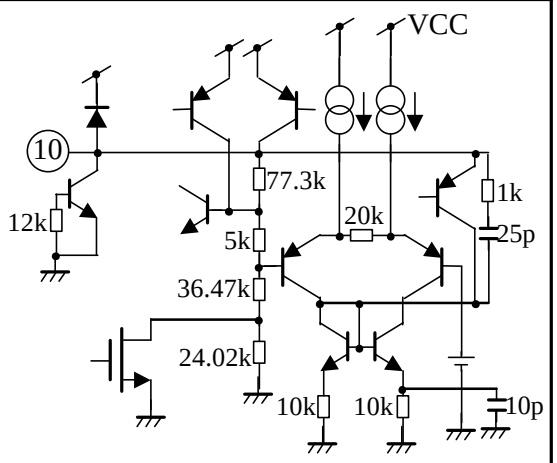
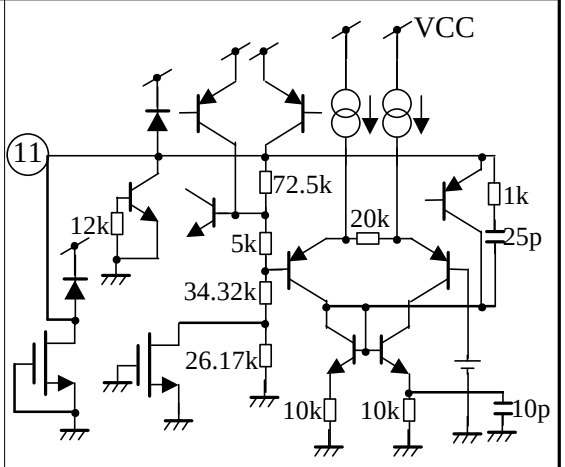
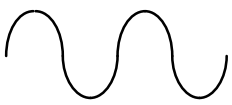
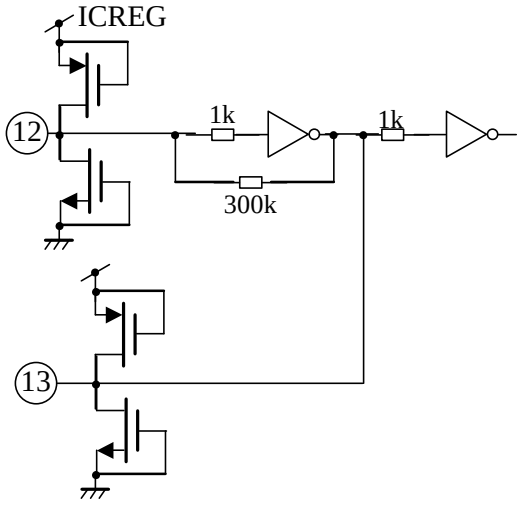
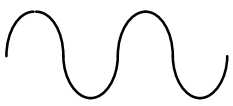
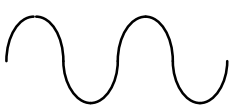
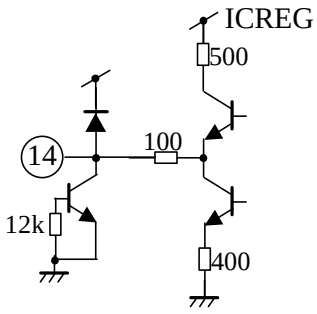
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Pin Name	Waveform and voltage	Function	Inner circuit
6	MCUREG	DC 2.8V	Regulator output pin for MCU	
7	RXREG	DC 2.8V	Regulator output pin for RX	
8	TXREG	DC 2.8V	Regulator output pin for TX	
9	VCC1	DC 4.5V	Power supply pin	

■ Technical Data

1.I/O block circuit diagrams and pin function descriptions (Continued)

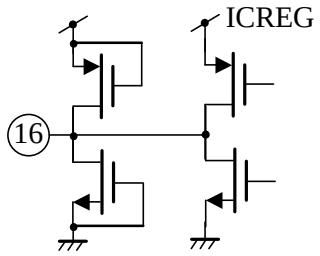
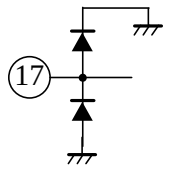
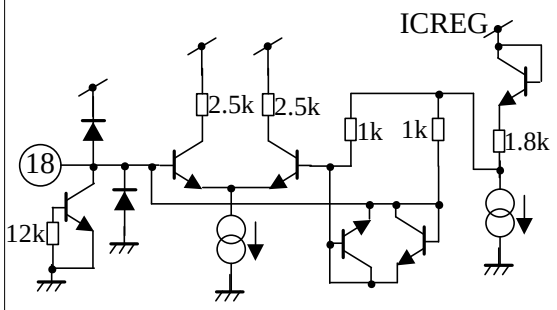
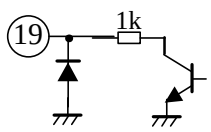
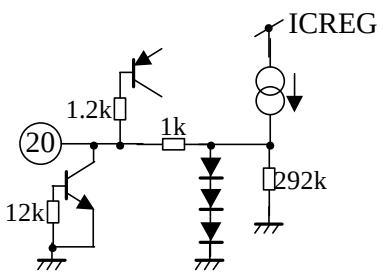
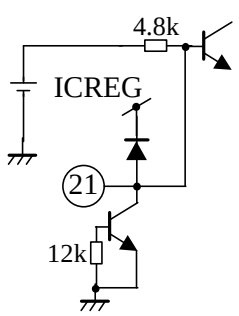
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Pin Name	Waveform and voltage	Function	Inner circuit
10	VCOREG	DC 2.9V	Regulator output pin for VCO	
11	ICREG	DC 2.8V	Regulator output pin for IC	
12	OSCI		Oscillator input pin	
13	OSCO		Oscillator output pin	
14	OSCOUT		Oscillator frequency/4 output	

■ Technical Data

1.I/O block circuit diagrams and pin function descriptions (Continued)

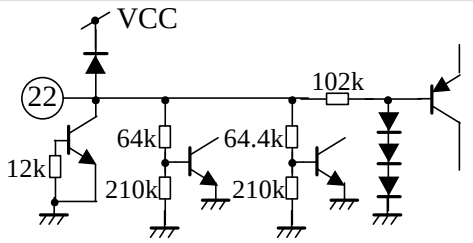
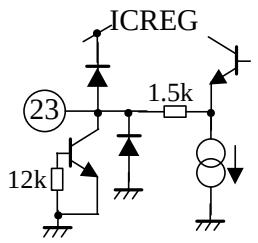
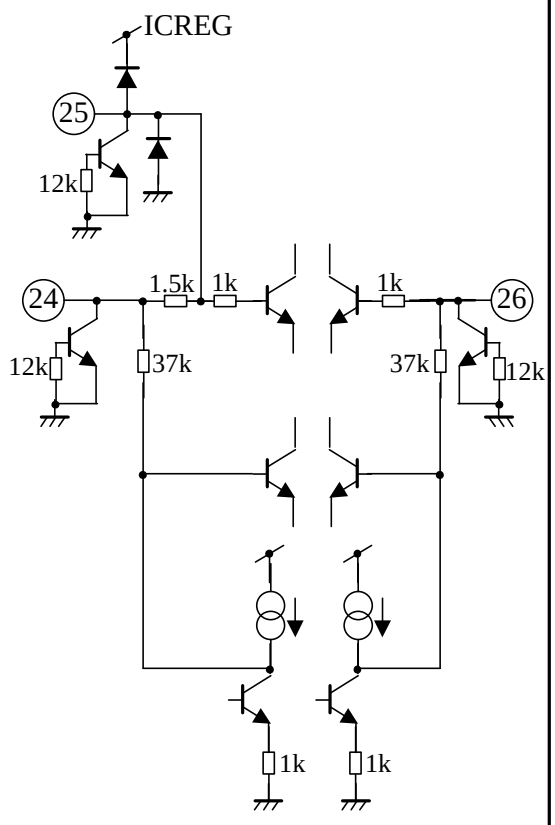
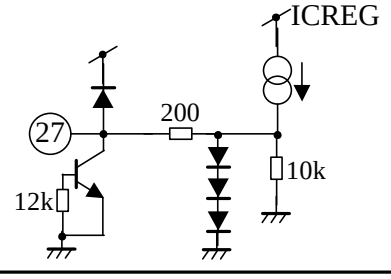
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Pin Name	Waveform and voltage	Function	Inner circuit
15	GND1	0V	Ground pin	
16	CP	DC Control Voltage	Phase comparator output pin	
17	VSS		Ground pin for Logic	
18	PLLIN	450MHz	PLL input pin	
19	SIGOUT	DC	LD,ND output pin	
20	NDET	With capacitor With no capacitor	Noise detection	
21	LIMIN	10.55MHz – 21.7MHz	IF amp1 input pin	

■ Technical Data

1.I/O block circuit diagrams and pin function descriptions (Continued)

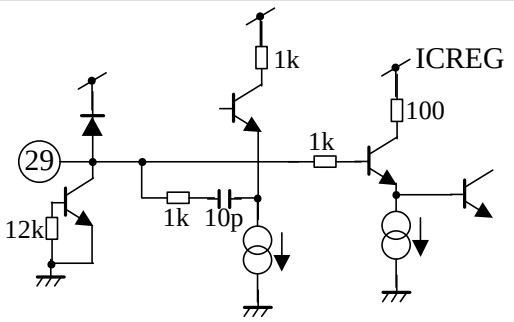
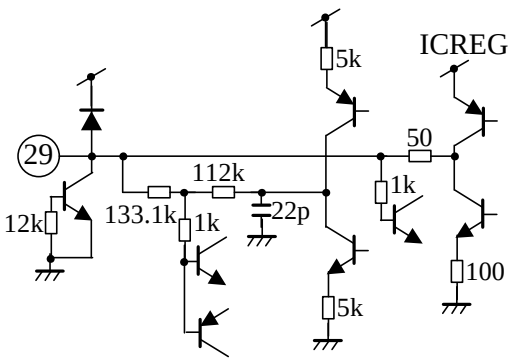
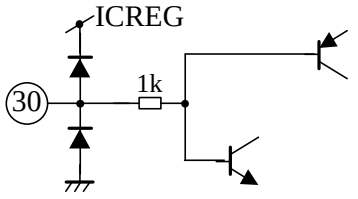
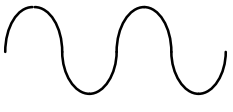
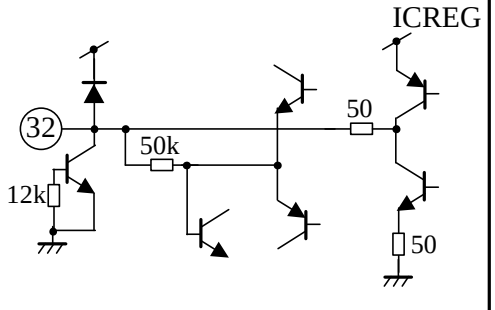
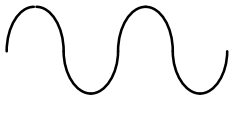
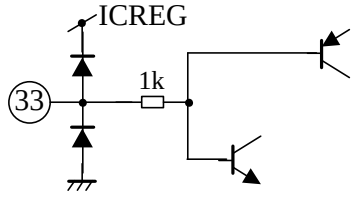
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Pin Name	Waveform and voltage	Function	Inner circuit
22	PCONT	DC	Power Off pin	
23	MIX2 OUT	450kHz	Mix2 output pin	
24	IFREF1	With capacitor With no capacitor	Coupling pin for IF amp2 feedback	
25	IFIN	450kHz	IF amp2 input pin	
26	IFREF2	With capacitor With no capacitor	Coupling pin for IF amp2 feedback	
27	RSSIDET	With capacitor With no capacitor	RSSI rectification pin	

■ Technical Data

1.I/O block circuit diagrams and pin function descriptions (Continued)

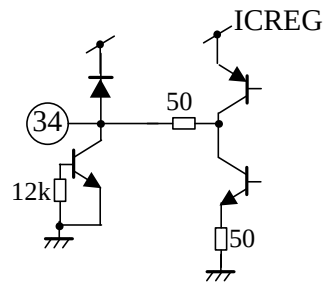
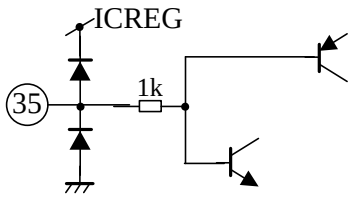
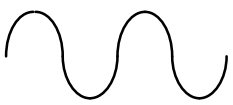
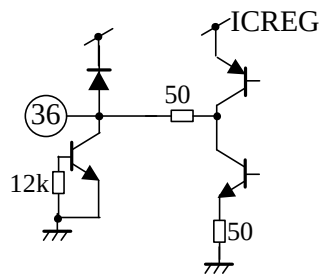
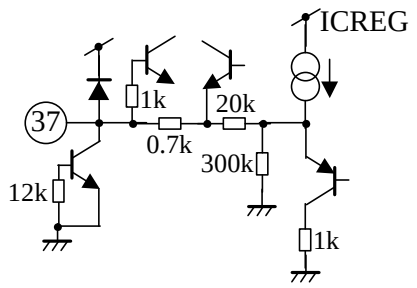
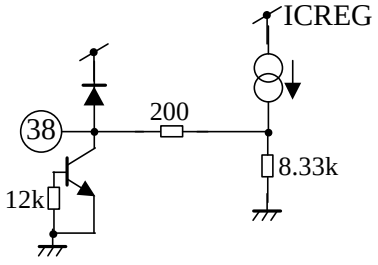
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Pin Name	Waveform and voltage	Function	Inner circuit
28	TANK		IF amp2 output pin	
29	DETOUT		FM Detector output pin	
30	NFIN		NF amp input pin	
31	PE		Zap current applied pin This is a pin for internal Zap adjustment Which is normally grounded	
32	NFOUT		NF amp output pin	
33	LPF1IN		LPF 1 input pin	

■ Technical Data

1.I/O block circuit diagrams and pin function descriptions (Continued)

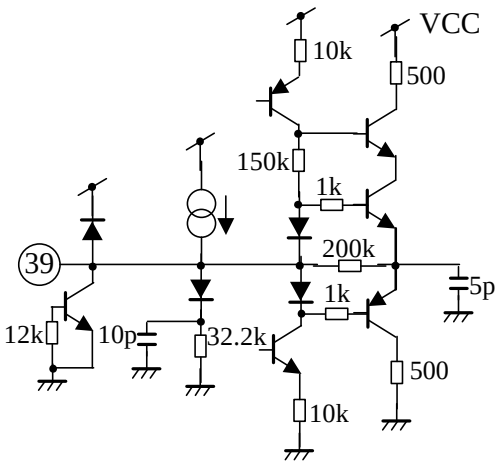
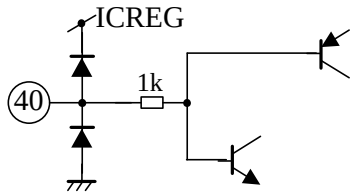
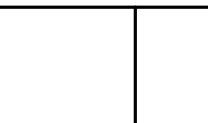
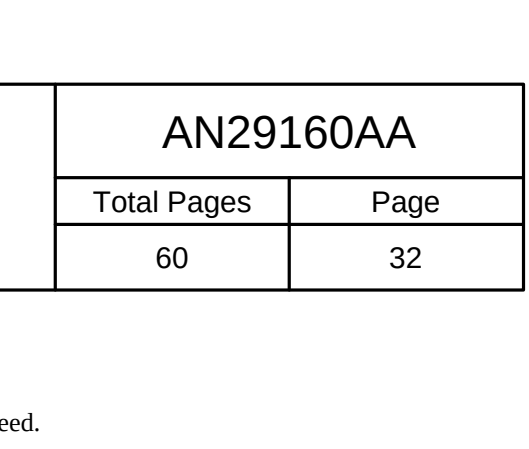
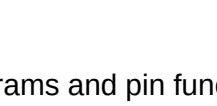
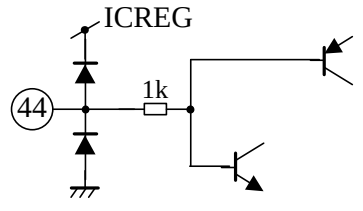
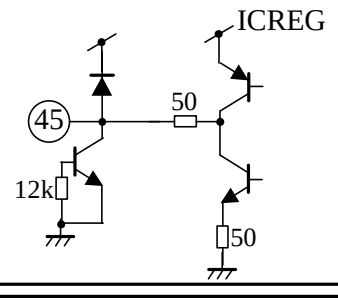
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Pin Name	Waveform and voltage	Function	Inner circuit
34	LPF1OUT		LPF1 output pin	
35	LPF2IN		LPF2 input pin	
36	LPF2OUT		LPF2 output pin Data amp input pin	
37	BREF	DC	Baseband reference pin	
38	VOXDET	With capacitor With no capacitor 	VOX Detection Output	

■ Technical Data

1.I/O block circuit diagrams and pin function descriptions (Continued)

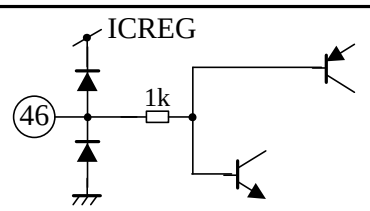
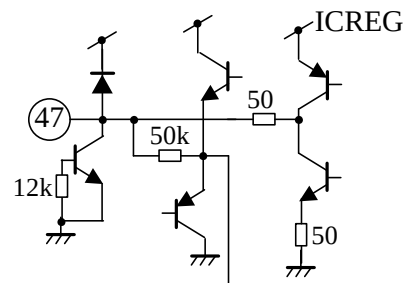
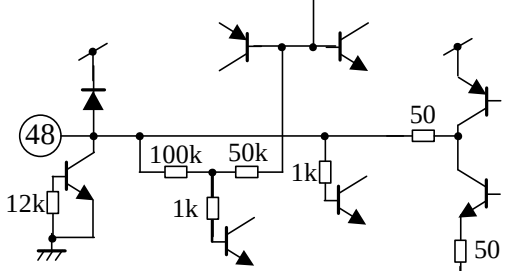
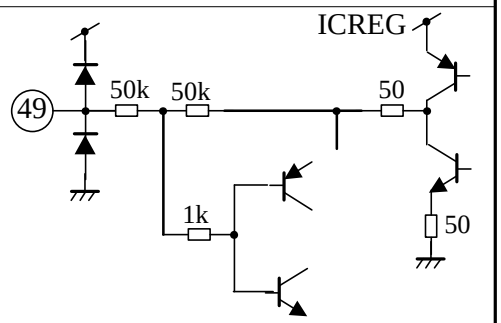
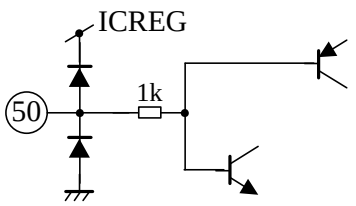
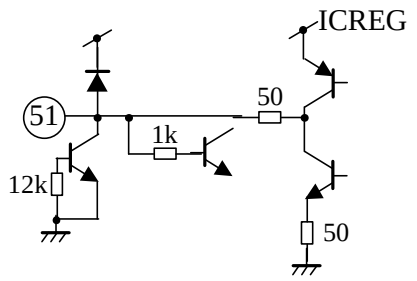
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Pin Name	Waveform and voltage	Function	Inner circuit
39	BGR	DC	BGR reference pin	
40	MICIN		Microphone amplifier input pin	
41	MIC OUT1		Microphone amplifier output pin	
43	MIC OUT2		Microphone amplifier mute output pin	
42	GND1	0V	Ground pin	
44	HPF1IN		HPF1 input pin	
45	HPF1OUT		HPF1 output pin	

■ Technical Data

1.I/O block circuit diagrams and pin function descriptions (Continued)

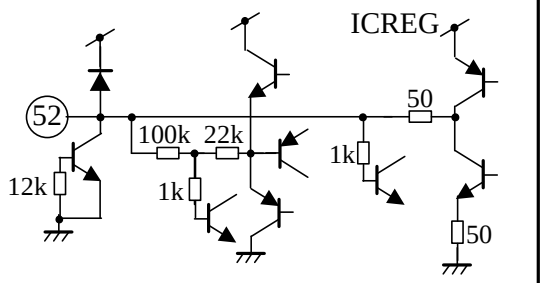
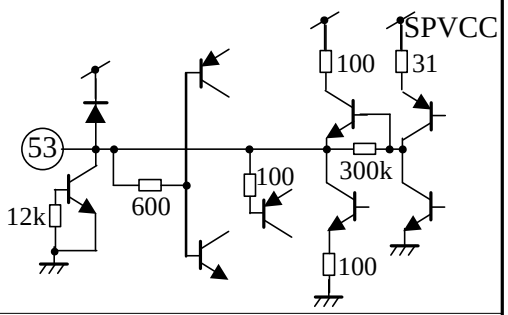
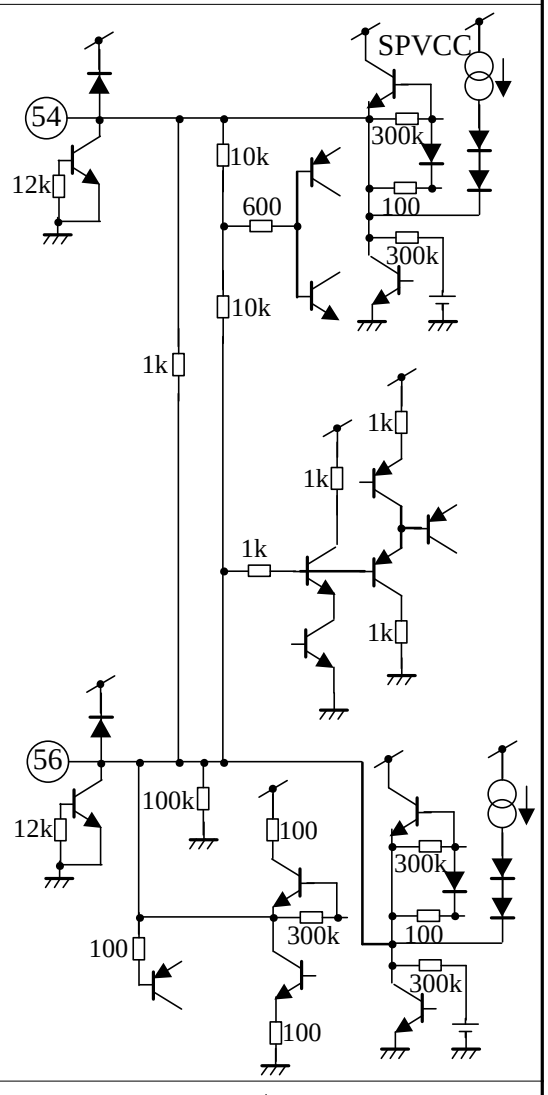
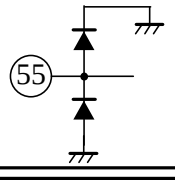
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Pin Name	Waveform and voltage	Function	Inner circuit
46	HPF2IN		HPF2 input pin	
47	HPF2OUT		HPF2 output pin Limiter input pin	
48	AMOUT		AF mute output pin	
49	TONE		Adder input pin	
50	SFIN		SF amp input pin	
51	SFOUT		SF amp output pin	

■ Technical Data

1.I/O block circuit diagrams and pin function descriptions (Continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

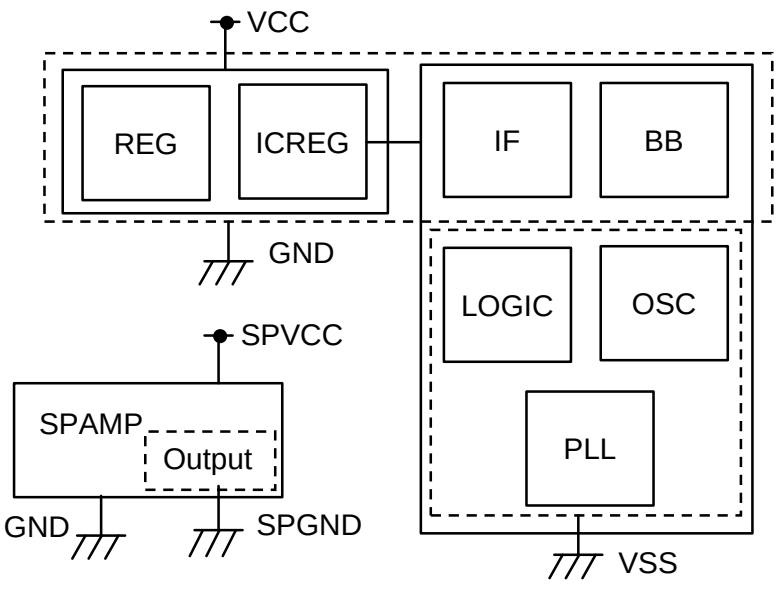
Pin No.	Pin Name	Waveform and voltage	Function	Inner circuit
52	EVOUT		Evol output pin	
53	SPIN		SP amp input pin	
54	SPOUT1		SP amp output pin	
56	SPOUT2		SP amp output pin	
55	SPGND	0V	Ground pin for SP amp	

■ Technical Data

2. Power Supply Block Assign

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

VCC		REG,ICREG
	GND	BB,IF,MICAMP,VOX, SPLATTER AMP
ICREG	VSS	DATA LATCH CONTROL, OSC,PLL
	SPGND	SPAMP (Output)
SPVCC	GND	SPAMP (Except Output)



■ Technical Data

3. Serial Data Control

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

(1) Data Registers and Addresses

LSB MSB

D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21	D22	D23
1	0	1	AFM	MICM	LIM	EV1	EV2	EV3	EV4	EV5	CHP	LDSW	CHPT	CNTT	ZMW	VSEL	RSEL	TSEL	ZAP0	ZAP1	ZAP2	ZAP3
1	1	0	SLP	PIF	PNSQ	PREF	PLPF	PHPF	PVOL	PADD	PVOX	PSP	SPPR	SPVR	PMIC	PSPL	PTXV	PRXV	PVCO			
1	1	1	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	ZEM	0	1	0	0			
1	0	0	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^{16}			

(2) Code allocation

Code			Control block	Function
D1	D2	D3		
1	0	1	Function control Test mode	Used for functional control. (Mute control, Volume control, etc.)
1	1	0	Power control	Used for power supply mode control.
1	1	1	Ref Counter	Used for phase comparison frequency setting.
1	0	0	CH Counter	Used for PLL output frequency setting.

■ Technical Data

3.Serial Control (Continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

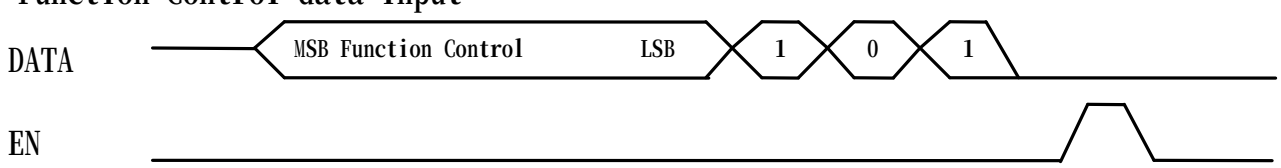
(3) Serial Data Input Procedure

◎ The shift register sequentially reads the data input status whenever the edge of CLK input rises.

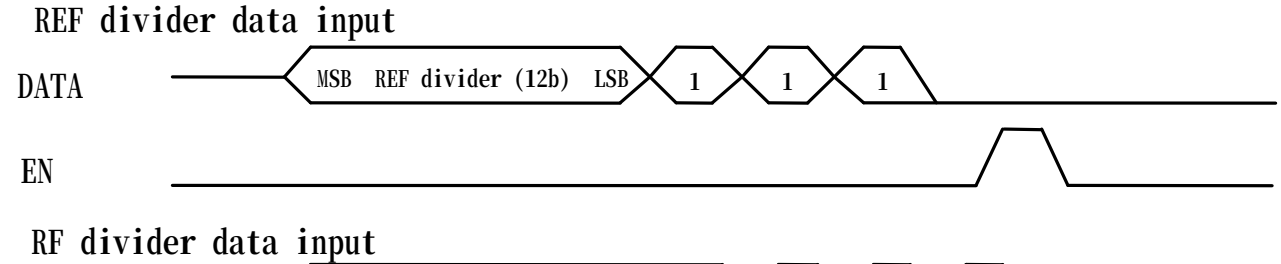
◎ All data is set at the rising edge of the D1 write CLK. The latch data that corresponds to the divider selected by D1, D2, and D3 is refreshed at the next rising edge of the EN.

◎ To enable the EN signal, set the DATA input status to zero.

1) Function Control data input

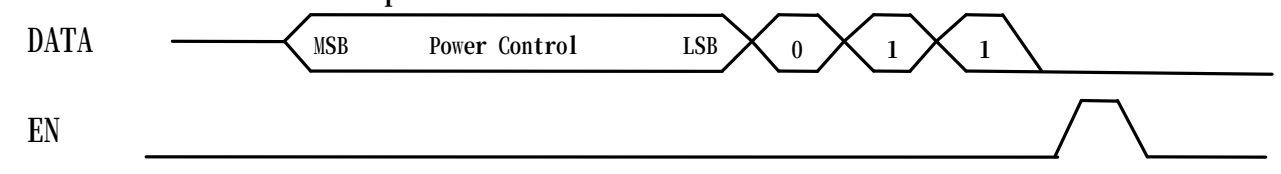


2) REF divider data input



3) RF divider data input

4) Power Control data input



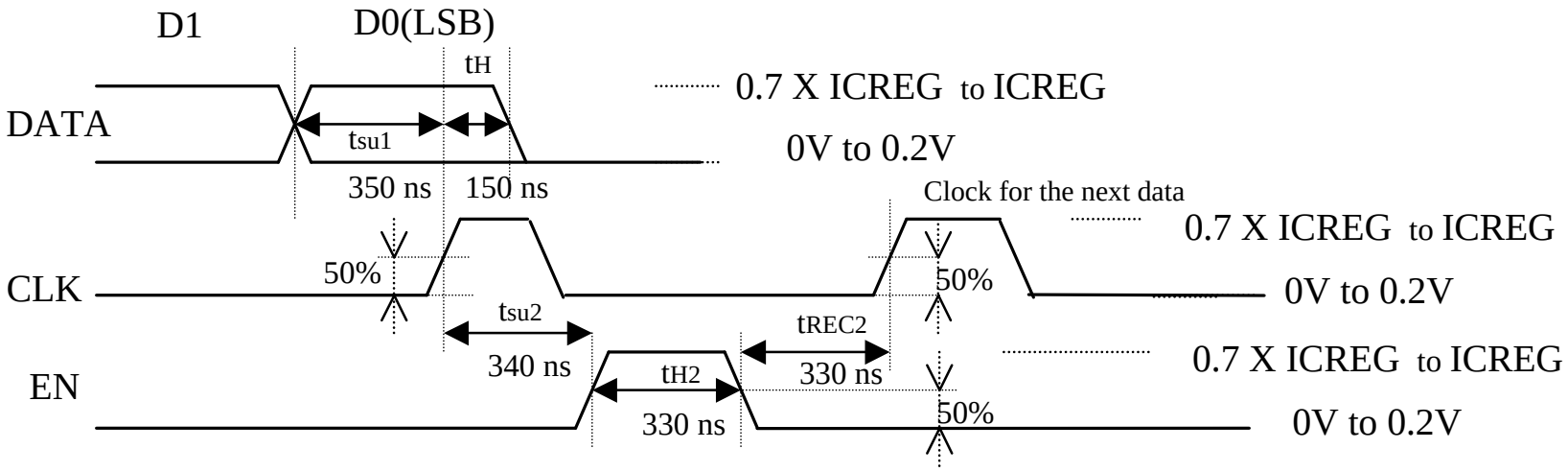
Note) Set the DATA, CLK, and EN pins to low level unless data is input to them.

■ Technical Data

3.Serial Control (Continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

(4) Serial Data Input Timing and Input Voltage



t_{su1}: Setup time (Data → Clock)≧350 ns
t_{su2}: Setup time (Clock → Enable)≧340 ns
t_H: Hold time (Clock → Data)≧150 ns
t_{REC2}: Recovery time (Enable falling edge→ Clock)≧330 ns
t_{H2}: Hold time (Enable rising edge→ Falling edge)≧330 ns

* The shift register sequentially reads the data input status whenever the edge of CLK input rises.

* To enable the EN signal, set the DATA input status to zero.

* Serial data must be input in sequence beginning with the MSB.

■ Technical Data

3.Serial Control (Continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

(5) Power Control Setting

Power Control

Control Block	PIN22	SERIAL DATA BIT																
		SLP	PIF	PNSQ	PREF	PLPF	PHPF	PVOL	PADD	PVOX	PSP	SPPR	SPVR	PMIC	PSPL	PTXV	PRXV	PVCO
BGR, REG Trim.	○																	
MCU REG	○																	
IF/BB REG	○																	
REF. OSC	○																	
1/4 DIVIDER	○																	
SERIAL DECODER	○																	
PLL COUNTER/CP		○																
IF AMP-1			○															
2nd MIX			○															
IF AMP-2			○															
RSSI			○															
FM DET			○*2		○*2													
NF AMP/SQ				○	○													
BREF, AFMUTE					○													
LPF					○	○												
HPF					○		○											
VOLUME					○			○										
ADDER					○				○									
VOX					○					○								
AF POWER AMP											○	○	○					
MIC AMP					○									○				
SPL FILTER					○*3										○*3			
TX REG																○		
RX REG																	○	
VCO REG																		○

*1) When SLP is "0", set LDSW to “0”.

*2) FMDET OUT Setting

PIF	PREF	FMDET OUT
1	1	Unmuted
0	1	Muted
0	0	OFF (HiZ)
1	0	Don't Use

*3) SFAMP OUT Setting

PSPL	PREF	SFAmp OUT
1	1	Unmuted
0	1	Muted
0	0	OFF (HiZ)
1	0	Don't Use

■ Technical Data

3.Serial Control (Continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

(6)Function Control Setting

Bit	Function	Control logic		Default setting *1	Note
		1	0		
AFM	AF MUTE	MUTE	PASS	1	
MICM	Micamp MUTE	MUTE	PASS	1	
LIM	TX Limiter control	Limiter	PASS	0	
CHP	PLL charge pump current capacity setting	100uA	800uA	0	
LDSW	Sigout pin output selection PLL LD /Noise squelch	NSQ	LD	0	
VSEL	VCO REG Output Voltage	4V	2.9V	0	
RSEL	RX REG Output Voltage	4V	2.8V	0	
TSEL	TXREG Output Voltage	4V	2.8V	0	
CHPT	Tr current capacity measurement	TEST	Normal	0 *2	for testing
CNTT	Used for counter test	TEST	Normal	0 *2	for testing
ZMW	Used for PROM writes	write	Normal	0 *2	for trimming
ZEM	Used for REG triming emulation	emulation	Normal	0 *2	for trimming

*1) Default setting is defined as initial value when pin 22 is set to high level from low level where IC is turned on.

*2) Set to 0 when the IC is in usual operation.

■ Technical Data

3. Serial Control (Continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

(7) EVOL Control Setting

STEP	SERIAL DATA BIT					Gain [dB]	Note
	EV1	EV2	EV3	EV4	EV5		
1	0	0	0	0	0	0	
2	1	0	0	0	0	-2	
3	0	1	0	0	0	-4	
4	1	1	0	0	0	-6	
5	0	0	1	0	0	-8	Standard Condition
6	1	0	1	0	0	-10	
7	0	1	1	0	0	-12	
8	1	1	1	0	0	-14	
9	0	0	0	1	0	-16	
10	1	0	0	1	0	-18	
11	0	1	0	1	0	-20	
12	1	1	0	1	0	-22	
13	0	0	1	1	0	-24	
14	1	0	1	1	0	-26	
15	0	1	1	1	0	-28	
16	1	1	1	1	0	-30	
17	0	0	0	0	1	-32	
18	1	0	0	0	1	-34	
19	0	1	0	0	1	-36	
20	1	1	0	0	1	-38	
21	0	0	1	0	1	-40	
22	1	0	1	0	1	-42	
23	0	1	1	0	1	-44	
24	1	1	1	1	1	Muted	
default	1	1	1	1	1	Muted	

■ Technical Data

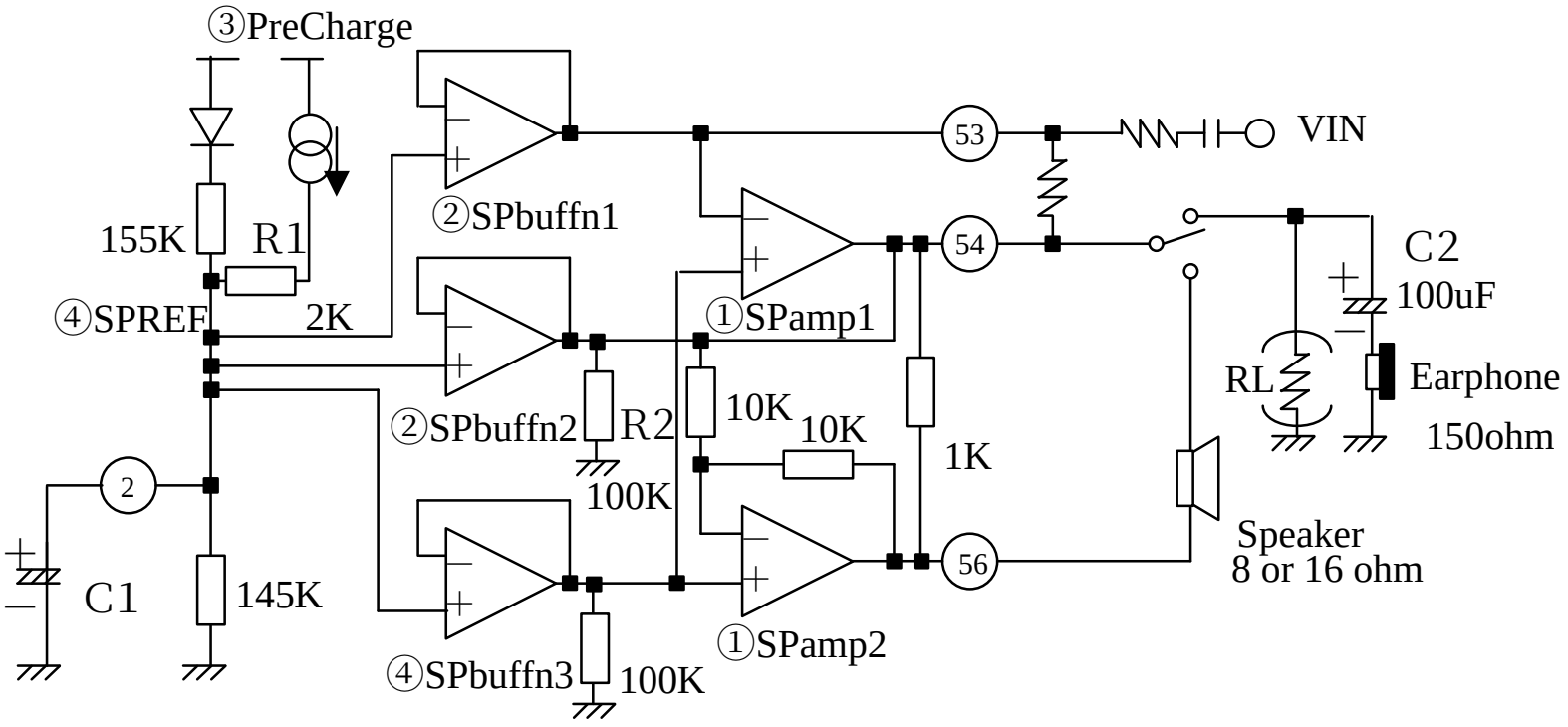
3. Serial Control (Continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

(8) SPamp Block Control

Circuit List

Circuit	Function
SPREF	for Reference Voltage
PREcharge	for External Capacitance Charge
SPbuffn1,2,3	for charge and Vref Buffer amp
SPamp1,2	for BTL amp



ON/OFF Circuit Group

No.	Block
①	SPAMP1 ,SPAMP2
②	SPbuffn1 , SPbuffn2
③	PREcharge
④	SPREF , Spbuffn3

SPREF Control

Control	Block	Function	Control Logic	
			1	0
SPVR	④	SPREF ON/OFF	Active	OFF

■ Technical Data

3. Serial Control (Continued)

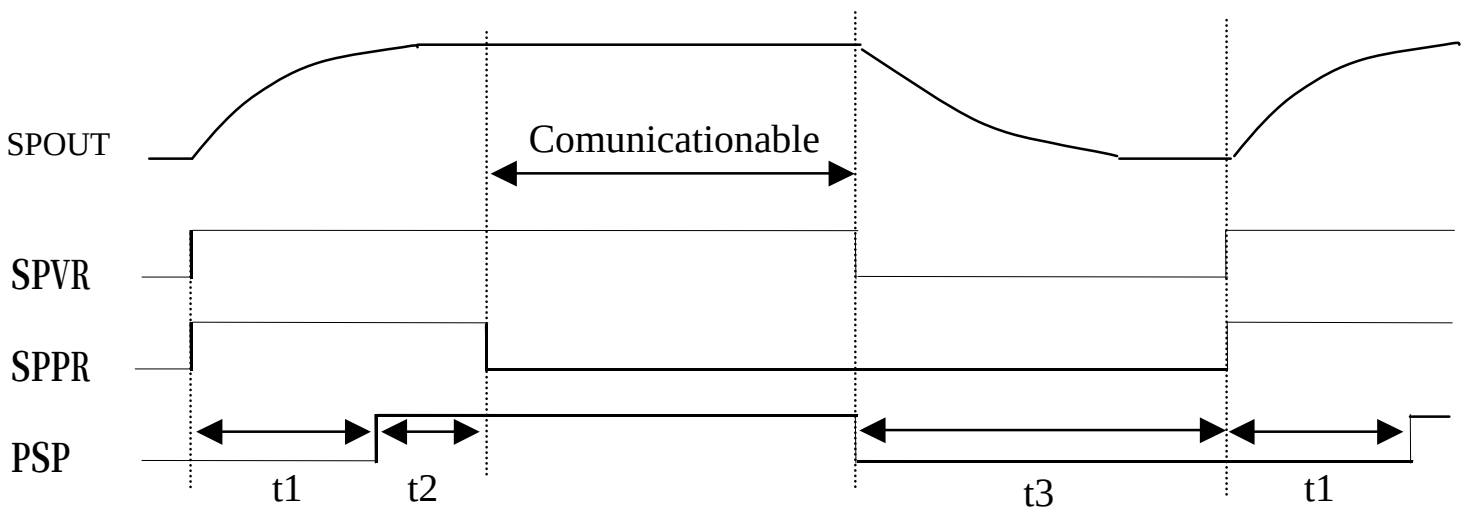
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Spamp,Spbuffn,PreCharge Control

Control	Block	Function
PSP	①,②	SP AMP & Buffer ON/OFF
SPPR	②,③	PreCharger & Buffer ON/OFF

Spamp,Spbuffn,PreCharge Control

PSP	SPPR	①	②	③
1	1	Active	OFF	Active
1	0	Active	OFF	OFF
0	1	OFF	Active	Active
0	0	OFF	OFF	OFF



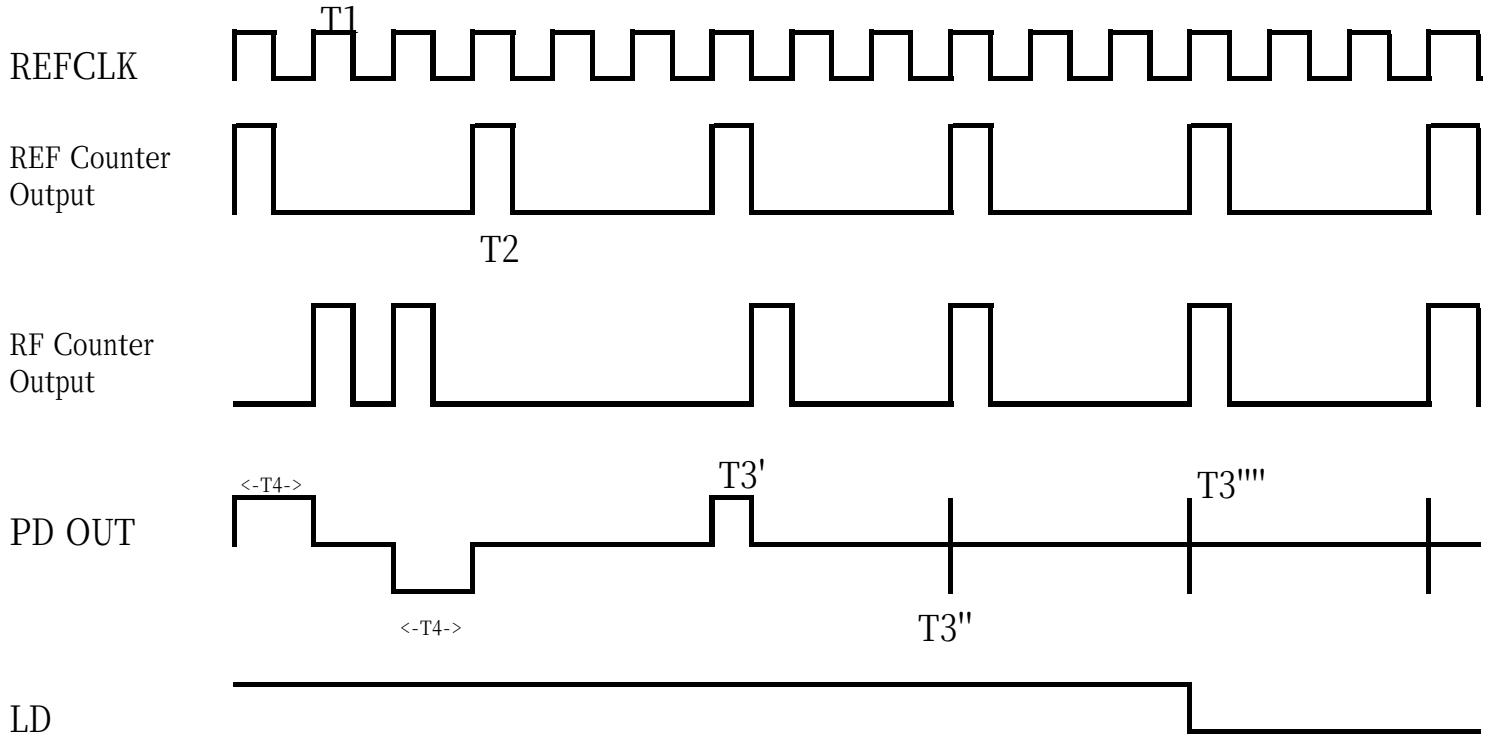
Recommended Power Sequence

No.	time	unit	Charge/Discharge Time
t1	50	ms	τ1=R1×C1
t2	>10	ms	-
t3	>2	s	τ3=(R2 // RL)×C2

■ Technical Data

4.Lock Detect

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.



Fref : REFCLK frequency
T1 = (1/2) *(1/Fref)
T2 = (1/2) *(1/Fref)
T3 < 1/Fref : PLL in Lock Condition
T4 > 1/Fref : PLL not in Lock Condition

*Locked Condition : IF T3 occurred 3 times, LD is High.

■ Technical Data

5.Counter Setting

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

(1) Counter Setting Method

The frequency dividing ratio is specified by a data-corresponding binary code.
The VCO oscillating frequency which corresponds to the reception or the transmission frequency f_{RF} is obtained from the following formula.

$$f_{RF} = P \times 2 \times [(f_{osc} / 2) \div R]$$

Here, R is the frequency dividing ratio of REF divider, P is the frequency dividing ratio of the RF divider, and f_{osc} is the reference oscillation frequency of the crystal oscillator.
Provided that the reference oscillation frequency (f_{xtal}) is 20.85 MHz, R is 1668 in order to obtain a reference frequency of 6.25 kHz (i.e., (f_{xtal}/2)÷R).

Possible Setting Range
Frequency dividing ratio of REF divider : R=5 to 4095
Frequency dividing ratio of RF divider : P=1056 to 131071

(2) Counter Default Setting when pin 22 is set to high level from low level

LSB MSB

Counter	Counter Default Setting																			
	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20			
REF Counter	0	0	0	1	0	1	0	0	1	1	0	0	-	-	-	-	-			
RF Counter	0	1	1	0	0	1	1	1	1	1	0	0	1	0	0	1	0			

REF counter: Frequency dividing ratio of 808×2
RX counter: Frequency dividing ratio of 37862×2

(3) Counter Setting Example

The following is an example of the counter setting to reception mode where RX PLL is active.

REF counter: 20.85 MHz → 6.25 kHz, R=1668
RF counter: $f_{(RF)}$= 462.7125 MHz → 6.25 kHz, P=37017

The following is the configuration of the serial data on each bit.

LSB MSB

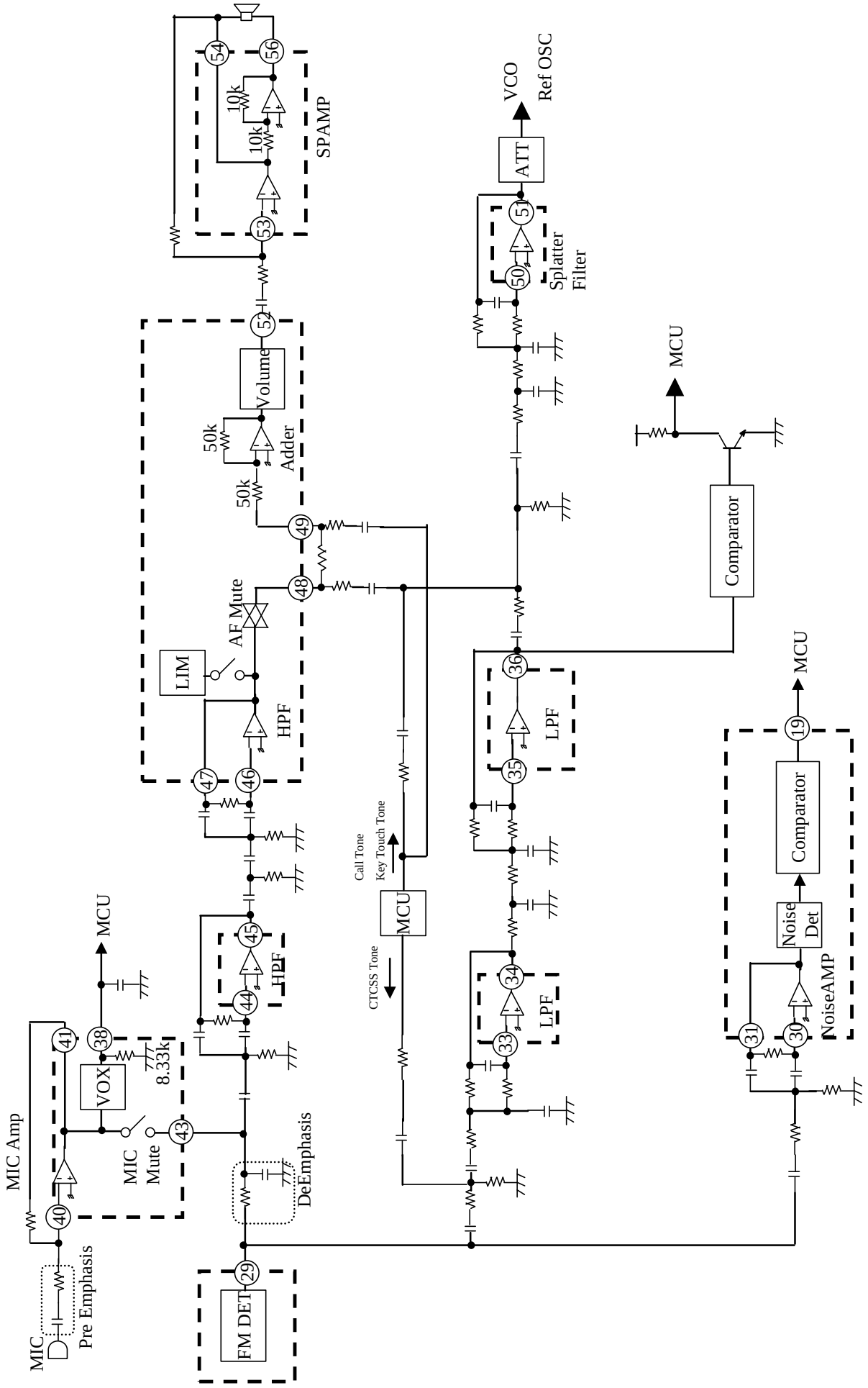
Counter	Counter Default Setting																			
	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20
REF Counter	1	1	1	0	0	1	0	0	0	0	1	0	1	1	0	-	-	-	-	-
RF Counter	1	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0	1	0

■ Technical Data

6. AF Signal Flow

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

(1) System Diagram



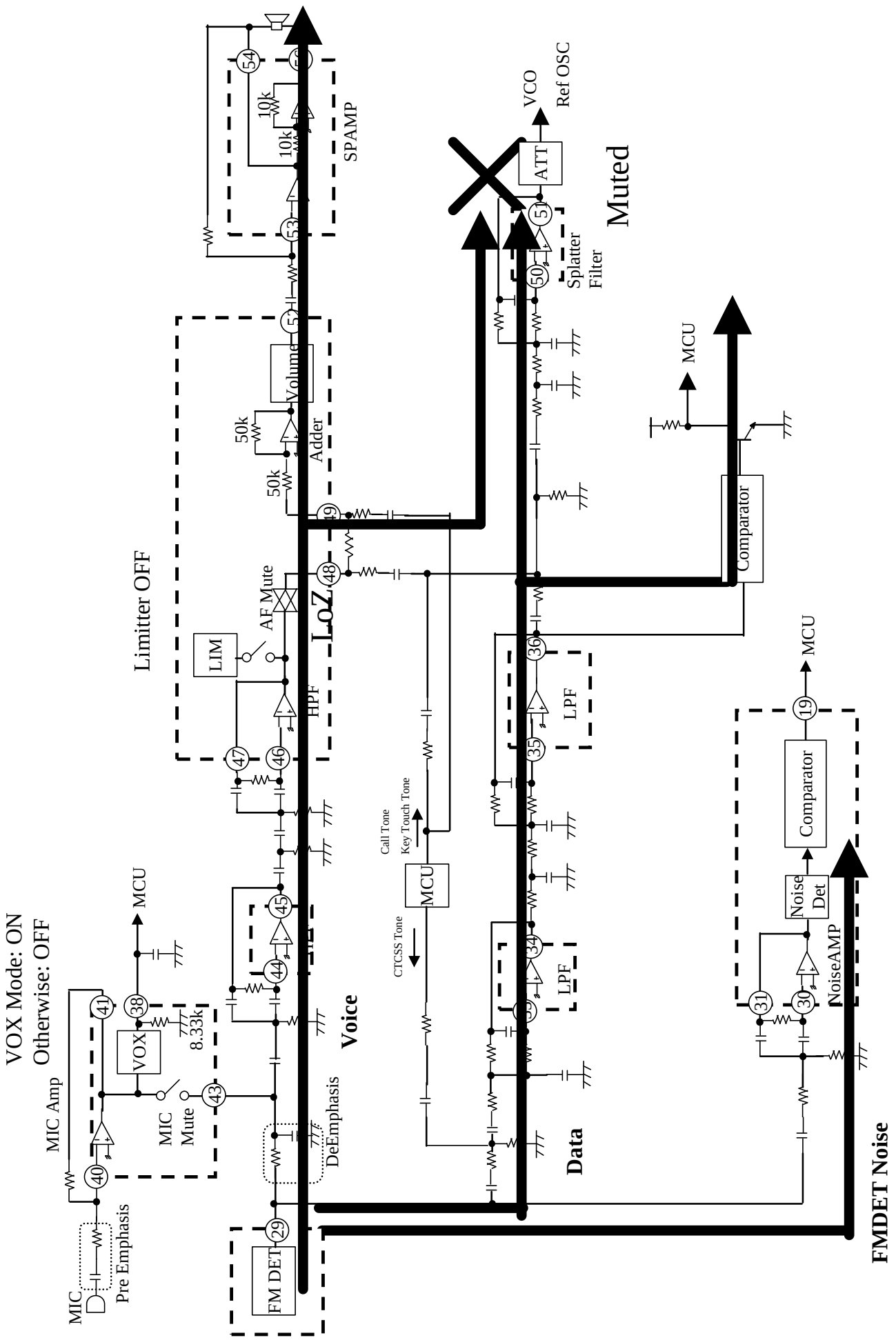
Established	Revised	

■ Technical Data

6. AF Signal Flow

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

(2) Reception Mode

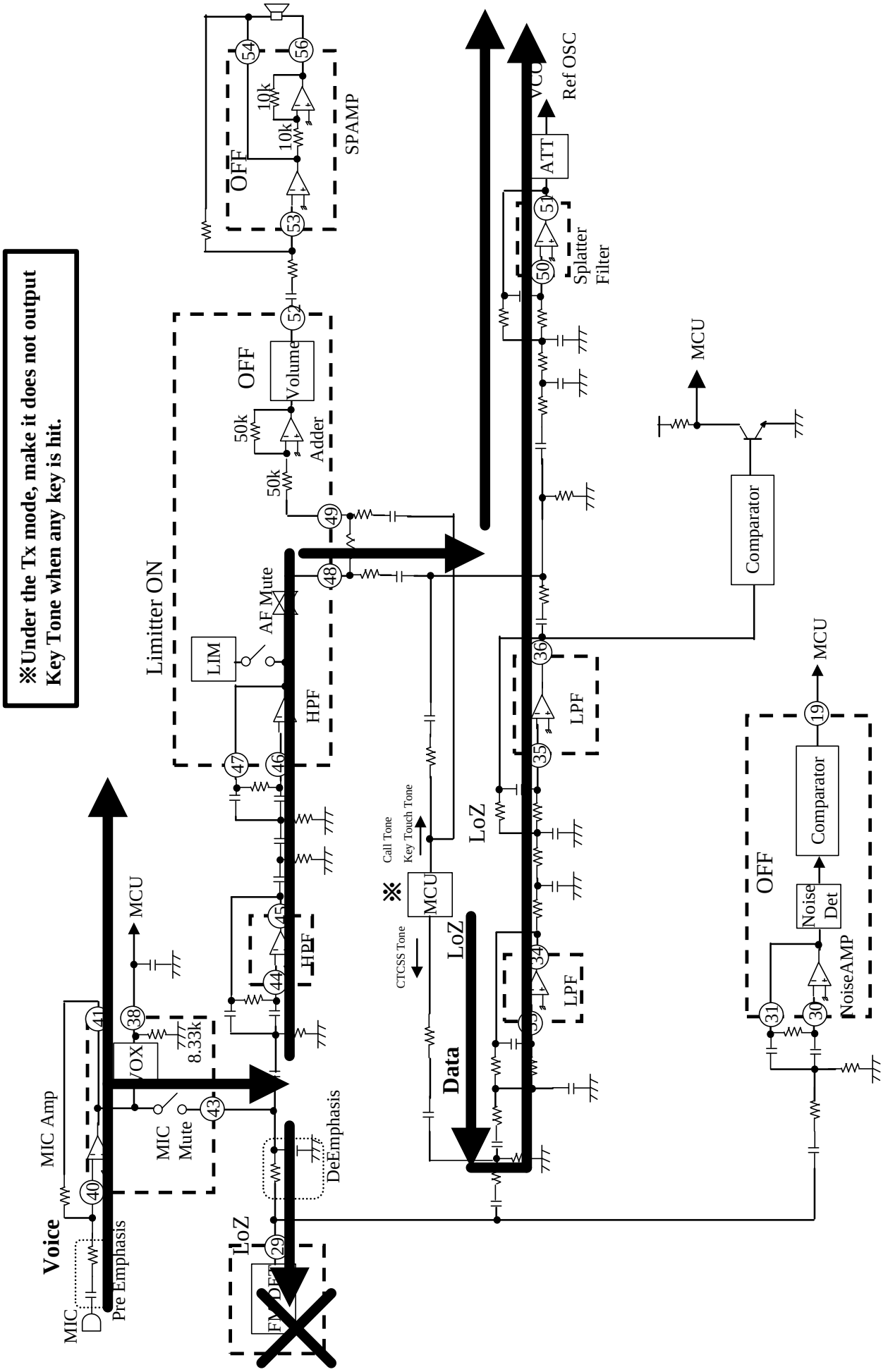


■ Technical Data

6. AF Signal Flow

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

(3) Transmission Mode

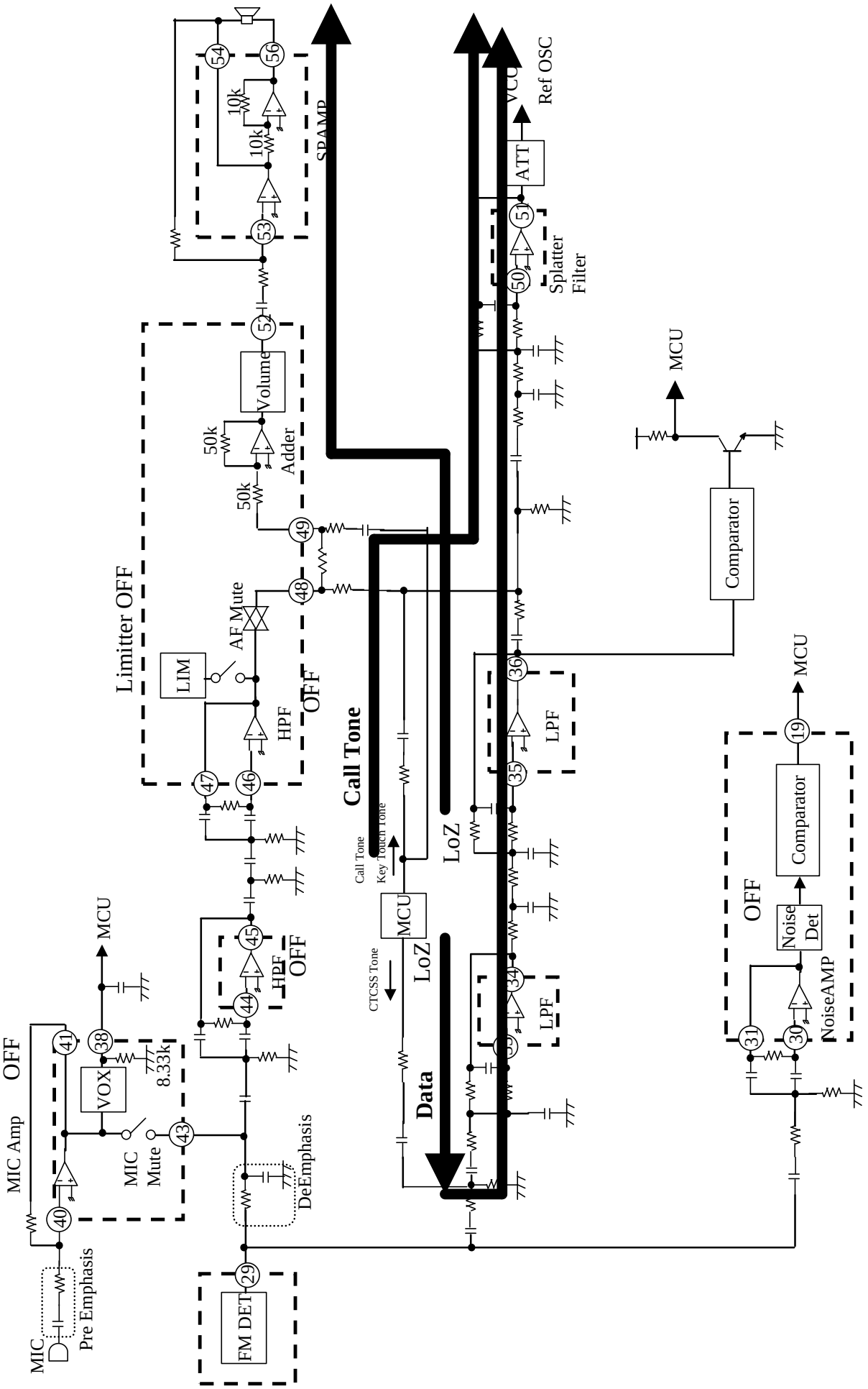


■ Technical Data

6. AF Signal Flow

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

(4) Call Tone Mode



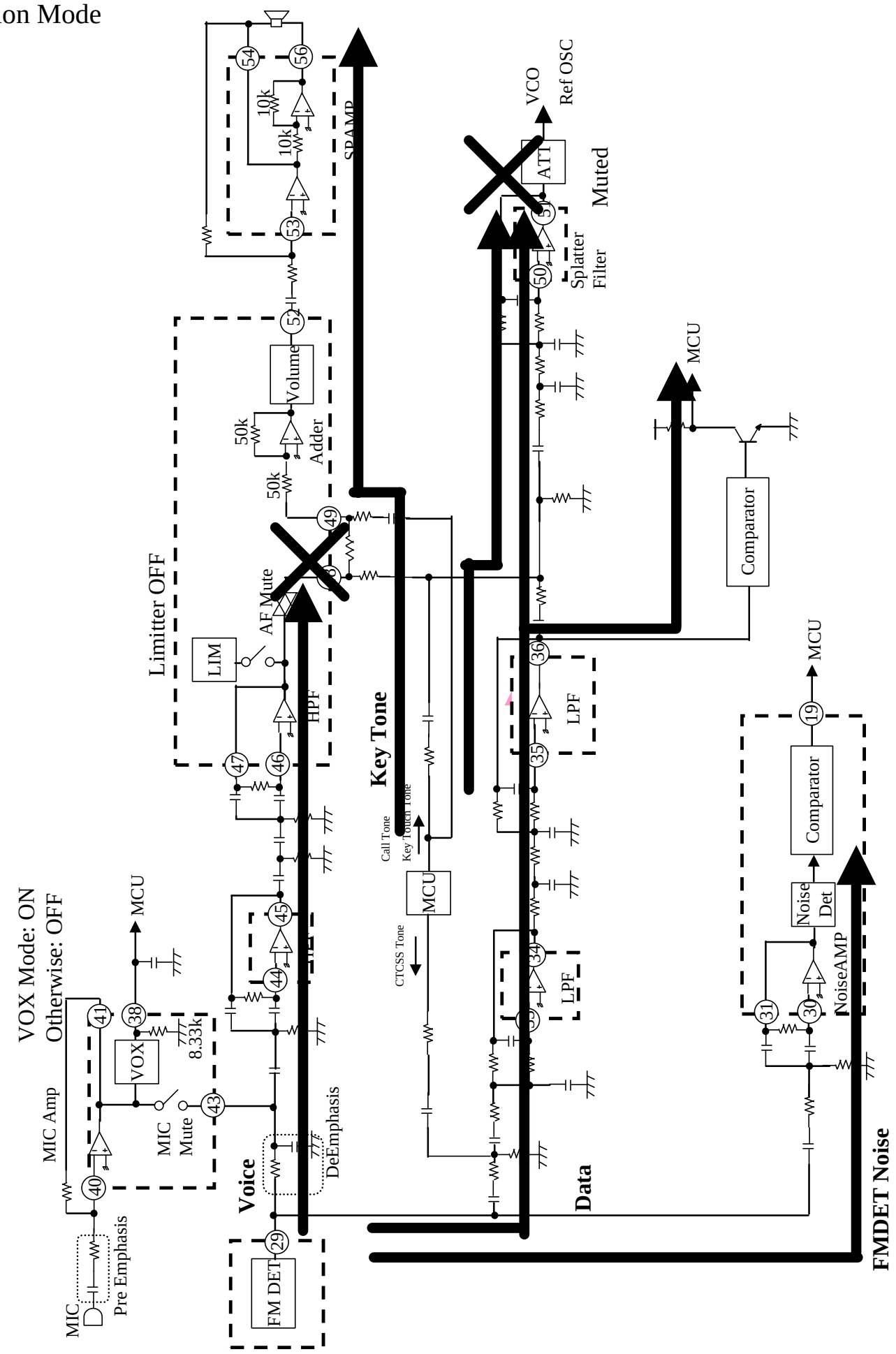
Established	Revised	

■ Technical Data

6. AF Signal Flow

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

(5) Key Touch in Reception Mode

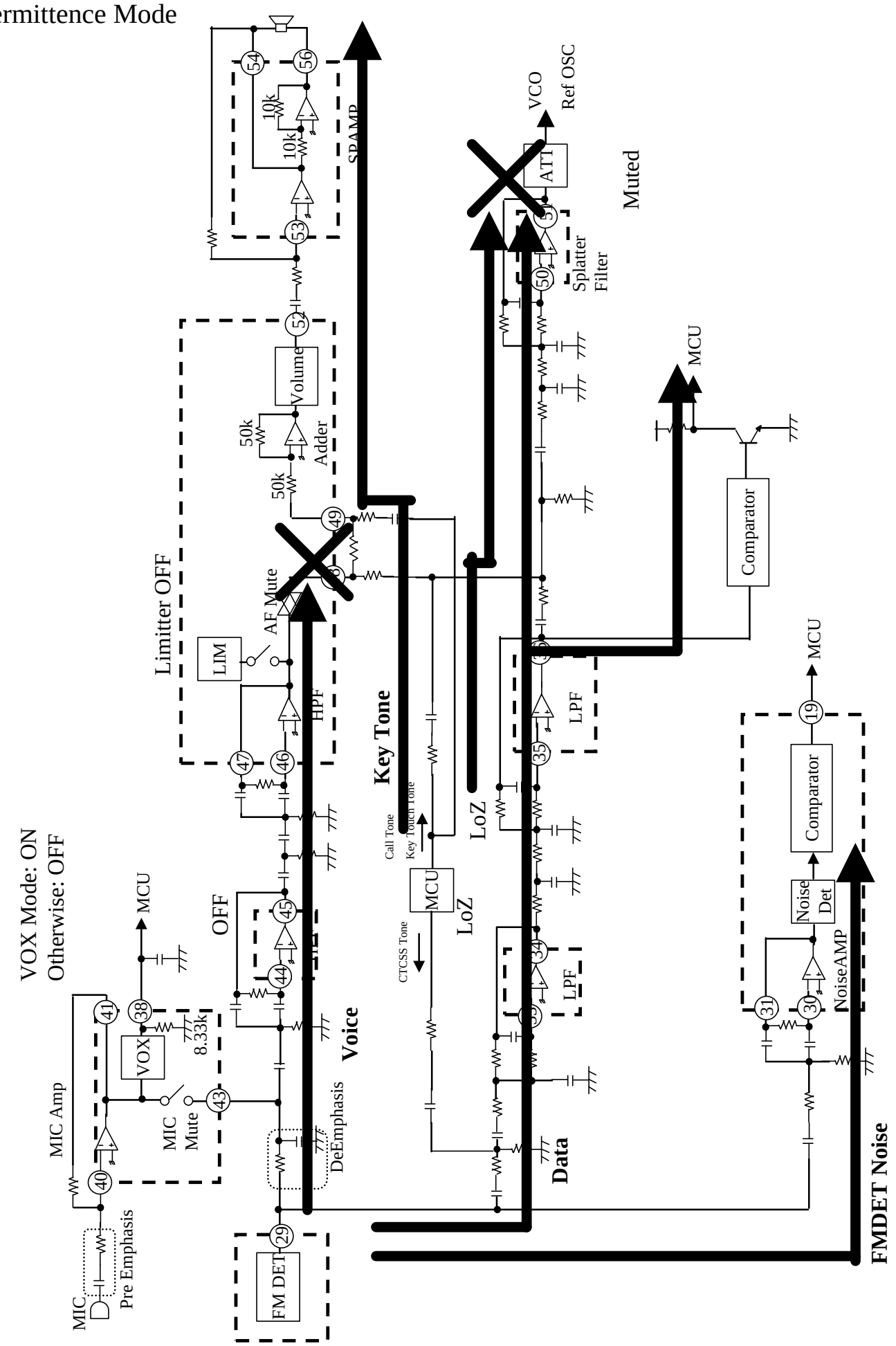


■ Technical Data

6. AF Signal Flow

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

(6) Key Touch in Intermittence Mode



Established	Revised	

■ Technical Data

6. AF Signal Flow

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

(7) Recommended Serial Data

(a) Reception Mode

MSB																						LSB
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
ZAP3	ZAP2	ZAP1	ZAP0	TSEL	RSEL	VSEL	ZMW	CNTT	CHPT	LDSW	CHP	EV5	EV4	EV3	EV2	EV1	LIM	MICM	AFM	1	0	1
0	0	0	0	*1	*1	*1	0	0	0	*1	1	*1	*1	*1	*1	*1	0	1	0	1	0	1
			PVCO	PRXV	PTXV	PSPL	PMIC	SPVR	SPPR	PSP	PVOX	PADD	PVOL	PHPF	PLPF	PREF	PNSQ	PIF	SLP	0	1	1
			1	1	0	0	*2	1	0	1	*2	1	1	1	1	1	1	1	1	0	1	1

(b) Transmission Mode

MSB																						LSB
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
ZAP3	ZAP2	ZAP1	ZAP0	TSEL	RSEL	VSEL	ZMW	CNTT	CHPT	LDSW	CHP	EV5	EV4	EV3	EV2	EV1	LIM	MICM	AFM	1	0	1
0	0	0	0	*1	*1	*1	0	0	0	0	1	1	1	1	1	1	1	0	0	1	0	1
			PVCO	PRXV	PTXV	PSPL	PMIC	SPVR	SPPR	PSP	PVOX	PADD	PVOL	PHPF	PLPF	PREF	PNSQ	PIF	SLP	0	1	1
			1	0	1	1	1	0	0	0	*2	1	0	1	1	1	0	0	1	0	1	1

(c) Call Tone Mode

MSB																						LSB
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
ZAP3	ZAP2	ZAP1	ZAP0	TSEL	RSEL	VSEL	ZMW	CNTT	CHPT	LDSW	CHP	EV5	EV4	EV3	EV2	EV1	LIM	MICM	AFM	1	0	1
0	0	0	0	*1	*1	*1	0	0	0	0	1	*1	*1	*1	*1	*1	0	1	1	1	0	1
			PVCO	PRXV	PTXV	PSPL	PMIC	SPVR	SPPR	PSP	PVOX	PADD	PVOL	PHPF	PLPF	PREF	PNSQ	PIF	SLP	0	1	1
			1	0	1	1	*2	1	0	1	*2	1	1	0	1	1	0	0	1	0	1	1

(d) Key touch in Reception Mode

MSB																						LSB
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
ZAP3	ZAP2	ZAP1	ZAP0	TSEL	RSEL	VSEL	ZMW	CNTT	CHPT	LDSW	CHP	EV5	EV4	EV3	EV2	EV1	LIM	MICM	AFM	1	0	1
0	0	0	0	*1	*1	*1	0	0	0	1	1	*1	*1	*1	*1	*1	0	1	1	1	0	1
			PVCO	PRXV	PTXV	PSPL	PMIC	SPVR	SPPR	PSP	PVOX	PADD	PVOL	PHPF	PLPF	PREF	PNSQ	PIF	SLP	0	1	1
			1	1	0	0	*2	1	0	1	*2	1	1	1	1	1	1	1	1	0	1	1

(e) Key touch in STBY Mode

MSB																						LSB
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
ZAP3	ZAP2	ZAP1	ZAP0	TSEL	RSEL	VSEL	ZMW	CNTT	CHPT	LDSW	CHP	EV5	EV4	EV3	EV2	EV1	LIM	MICM	AFM	1	0	1
0	0	0	0	*1	*1	*1	0	0	0	1	1	*1	*1	*1	*1	*1	0	1	1	1	0	1
			PVCO	PRXV	PTXV	PSPL	PMIC	SPVR	SPPR	PSP	PVOX	PADD	PVOL	PHPF	PLPF	PREF	PNSQ	PIF	SLP	0	1	1
			1	1	0	0	*2	1	0	1	*2	1	1	0	1	1	1	1	1	0	1	1

Note)

*1: Set as you like.

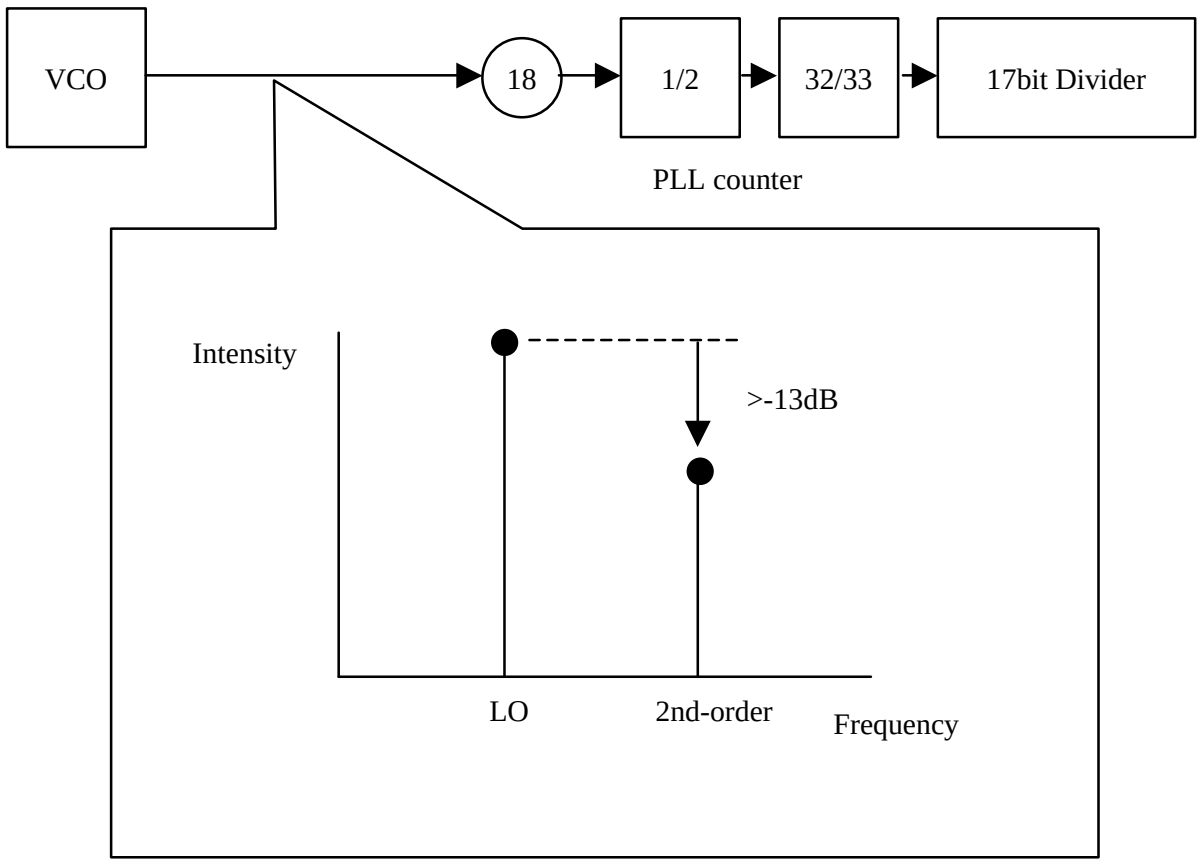
*2: Set these bits to "1" in hands-free Mode.

■ Technical Data

7. Cautions about secondary harmonics level of VCO output

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Please set secondary harmonics as -13dB or less to a LO signal level.
When secondary harmonics are larger than -13dB, PLL counter may incorrect-operate.
It is because counter receives secondary harmonics.



別紙A3シート参照

別紙A3シート参照

別紙A3シート参照

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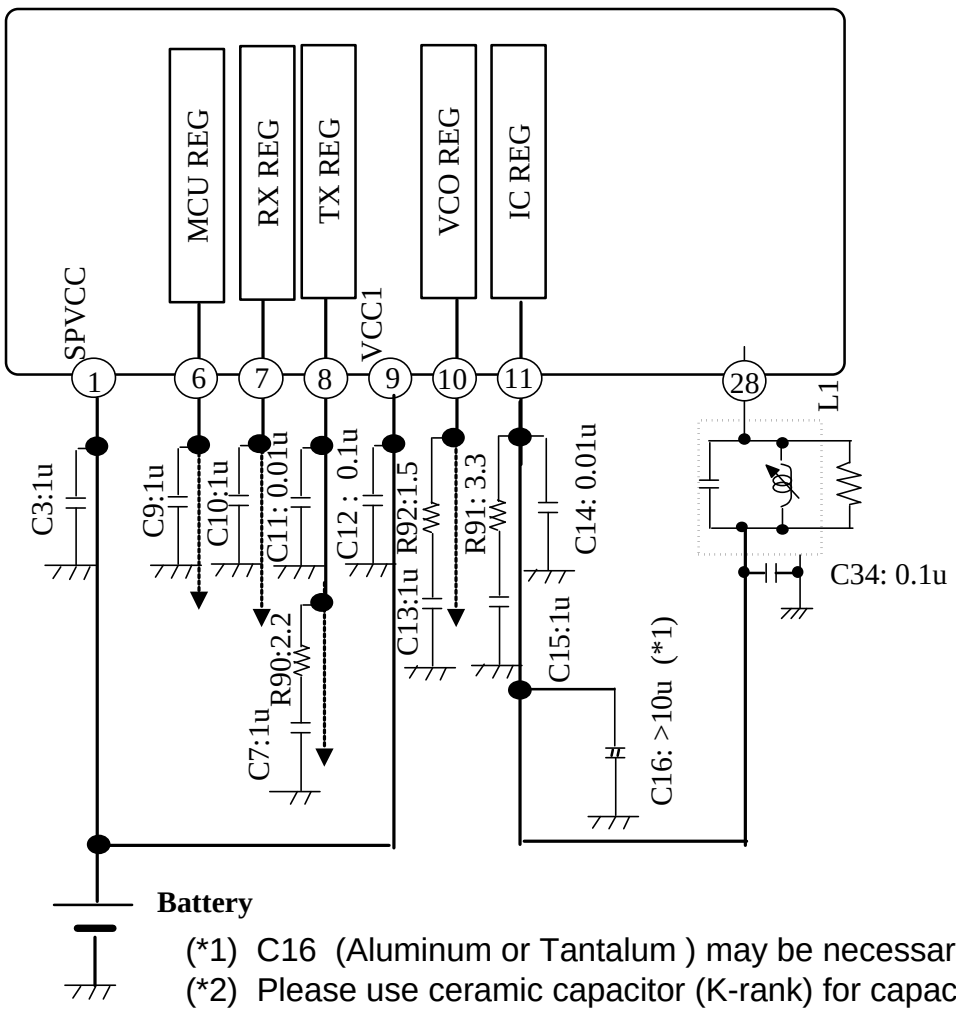
■ Technical Data

9. Caution about Regulators

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.



(*1) C16 (Aluminum or Tantalum) may be necessary to better receiving sensitivity.
(*2) Please use ceramic capacitor (K-rank) for capacitors except C16.

Use of unsuitable external parts of VCC terminal and Regulator outputs may cause oscillation.
Set these parts to above recommended values and set current load to values described in below table.
Please check the further characteristic in set PCB in use.

	External current load range without oscillation
RXREG	0 to 20mA
MCUREG	0 to 20mA
VCOREG	0 to 20mA
TXREG	0 to 100mA
ICREG	0 to 3mA (RX Mode) / 0 to 4mA (TX Mode)

■ Usage Notes

●Pins of this IC should be free of output-VCC short or output-GND short.

●Especially, Pin54 (SPAMP OUT1) and Pin56 (SPAMP OUT2) may be damaged due to output-VCC short.
Make sure that the IC is free of output-VCC short.

●Connect the cooling fin with the GND potential.

●Design the heat radiation carefully when you take out high power at high VCC .